LEVEL II

September 1981 MRDC41070.9QR

LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

Quarterly Technical Report No. 3

For Period 02/01/81 through 04/30/81

Contract No. F49620-80-C-0101

Project No. 3384-4

ROCKWELL INTERNATIONAL
Microelectronics Research and Development Center
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Sponsored by:

Advanced Research Projects Agency (DOD)
ARPA Order No. 3384-4
Monitored by AFOSR under Contract No. F49620-80-C-0101

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER AFOSR-TR- 81-0745	2. GOVT ACCESSION NO. AD-A107623
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) LSI/VLSI ION IMPLANTED GaAs IC PROCESSING	5. TYPE OF REPORT & PERIOD COVERED Quarterly Technical Report 02/01/81 through 04/30/81
	6. PERFORMING ORG. REPORT NUMBER MRDC41070.9QR
7. AUTHOR(s) R. Zucca, B. M. Welch, C. P. Lee, Y. D. Shen, P. Asbeck, C. G. Kirkpatrick, A. Firstenberg, G. Kaelin	8. CONTRACT OR GRANT NUMBER(s) F49620-80-C-0101
9. PERFORMING ORGANIZATION NAME AND ADDRESS ROCKWELL INTERNATIONAL/Microelectronics Research and Development Center 1049 Camino dos Rios Thousand Oaks, CA 91360	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F 3384/04 ARPA Order No. 3384-4
11. CONTROLLING OFFICE NAME AND ADDRESS Advanced Research Projects Agency (DOD) 1400 Wilson Boulevard Arlington, VA 22209	12. REPORT DATE September 1981
	13. NUMBER OF PAGES 69
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Air Force Office of Scientific Research /NE Bolling Air Force Base Washington, DC 20332	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Semi-insulating	High Speed Logic
Ion Implantation	GaAs
IC	FET
Integrated Circuits	MESFET

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the third quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. During this reporting period, the digitization of mask set AR6 has been completed. This mask set contains an SD^{2}FL 8 x 8 bit parallel multiplier, and a 7/8 bit programmable code generator. At the end of the quarter the mask set was being fabricated, and the masks were expected from the vendor.

Work has continued delving into those factors affecting the reproducibility of the n- active layer. Analysis of V_p and σV_p as a function of time has revealed

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substantial improvements in the reproducibility of these values. The specific effects of a number of parameters affecting V_p are being investigated. Detailed examination of the effects of room temperature dual implantation of Si with As has been completed at Caltech in an effort to enhance the peak doping levels feasible for this dopant.

Experiments started in the previous quarter and designed to evaluate the third, n^{++}, implant step have demonstrated an improvement in circuit performance attributed to the lower FET source resistance. One of the main yield limiting factors on the 8 x 8 multiplier (1000 gates) circuits has been identified as random shorts between second level metal power supply lines. Evaporation and magnetron sputtering deposition techniques for the second level metal are being compared in order to determine which technique is more immune to metal splattering and photoresist defects.

Reliability studies on GaAs integrated circuits have been started on ‡80/82 MSI (~60 gate) circuit. This packaged circuit has been tested under bias for 1700 hours at 125°C in air without failure.

Two dimensional numerical calculations have begun at North Carolina State University for the FET structures used in this program. Work on incorporating a Monte Carlo calculation, and time dependent (transient) analysis is in progress.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor, with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred H. Eisen. The principal investigators for each organization are:

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TECHNICAL SUMMARY

This report covers the third quarter of a program on LSI/VLSI ion implanted planar GaAs integrated circuit processing. The goal of this program is to realize the full potential of GaAs digital integrated circuits employing depletion mode MESFETs by developing the necessary processing methods and material capabilities to extend device complexity to VLSI. In the third quarter the digitization of mask set AR6 was completed. Masks are expected from the vendor shortly. Evaluation of refinements in the fabrication process aimed at improving reliability has continued, while evaluation of circuit reliability has been started. The work carried by the subcontractors (Caltech, North Carolina State University, and Crystal Specialties) is beginning to produce results.

Semi-Insulating Materials and Ion Implantation

During this reporting period, work has continued investigating those factors affecting the reproducibility of the n^- active layer. Analysis of V_p and σ_{Vp} as a function of time has revealed substantial improvements in the reproducibility of these values. The specific effects of a number of parameters affecting V_p, such as Si_3N_4 thickness before and after implant, implantation energy, and substrate material type are being investigated. The impact of using LEC GaAs, which has demonstrated good uniformity in addition to reproducibility, has been investigated.

In this same period, research at Caltech has concentrated on more detailed examination of the effects of room temperature dual implantation of

Si with As in an effort to enhance the peak doping levels feasible for this dopant. Detailed profiling of carrier concentrations and mobilities was carried out at Caltech for samples prepared at Rockwell. Co-implanted As does not appear to have an effect on Si activation except in the transition region of $10^{14}/cm^2$, where a complex behavior is observed.

Process Stabilization

Experiments started in the previous quarter and designed to evaluate the third, n^{++}, implant step have demonstrated an improvement in circuit performance attributed to reduced FET source resistance. Ring oscillators with a range (60 to 400 Ω/□) of sheet carrier concentrations under the ohmic contact regions have been evaluated. Gate propagation delays were found to decrease with sheet carrier concentrations in the n^{++} implant regions.

One of the main yield limiting factors on the 8 x 8 multiplier (1000 gates) circuits has been identified as random shorts between second level metal power supply lines. Splattering of the evaporated metal and/or random photoresist defects appear to be the primary cause of these metal shorts. Alternate approaches comparing evaporation and magnetron sputtering deposition techniques for the second level metal are being evaluated.

Reliability studies on GaAs integrated circuits have been started on ÷80/82 MSI (~60 gate) circuit (fabricated under an IR&D program). This packaged circuit has been tested under bias for 1700 hours at 125°C in air without failure. Clock frequencies of 800 MHz were maintained throughout the test with only minor changes observed in I_{SS} and I_{DD} currents.

Circuit Design

The digitization of mask set AR6 has been completed. This mask set contains an SD^{2}FL 8 x 8 bit parallel multiplier, and a 7/8 bit programmable code generator. At the end of this reporting period, mask set fabrication was in progress and nearly completed.

MESFET Device Modeling

Two dimensional numerical calculations have begun at North Carolina State University for the FET structures used in this program. Preliminary calculations were made using a uniform carrier density profile and were followed by calculations using a Gaussian profile to simulate an ion implantation profile. Good agreement with experimental data was obtained for the static characteristics, with further improvement expected for a more accurate carrier concentration profile. Work on incorporating a Monte Carlo calculation, and time dependent (transient) analysis is in progress.

1.0 INTRODUCTION

This report covers the third quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. The main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication techniques as well as material growth, preparation and selection. The principal goal is to improve material and processing capabilities so that large wafers (over 2 inch diameter) can be processed, in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program is also directed toward the investigation of circuit reliability, and the development of processing techniques and circuit designs capable of attaining the highest reliability. Circuit design advancements are also explored with the introduction and implementation of multilevel logic circuits. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

While equipment preparation for processing of large wafer continues, several aspects of process development have received attention. The work in this area is aimed at improving device performance, process yield, and circuit reliability, and it is supported by a sustained effort in semi-insulating substrate analysis and ion implantation development. As a result of these combined activities, improvements in reproducibility of FET threshold voltage

have been observed, reliability data have shown improved results in terms of operation at elevated temperature and time without failure. Ring oscillator data have reflected modest but yet valuable speed improvements as a result of process refinements.

Design and digitizing of mask set AR6 was completed before the end of the third quarter. This mask set contains an 8x8 bit parallel multiplexer implemented with SD^2FL, and 8-stage and 7-stage code generators implemented with 2 level (OR/NAND) SDFL. Wafer fabrication of this mask set will be started in the fourth quarter.

The subcontractor activity is beginning to obtain results. The research team at the California Institute of Technology has completed a study on co-implantations of Si and As into semi-insulating GaAs. The team at North Carolina State University has already produced results from their modeling of the low threshold GaAs MESFET used in the SDFL circuits.

2.0 SEMI-INSULATING MATERIAL AND ION IMPLANTATION

Activities during this quarter have emphasized the steady progress being made in doping profile reproducibility. This progress reflects in improved FET threshold voltage reproducibility. Data in Sec. 2.1 statistically document this progress. As improvements are made, successively finer scales of variations become observable. Cap thickness and cap stress effects are discussed in Sec. 2.1.

Attempts to improve the activation of high dose implants to raise the free carrier concentration above the apparent 2×10^{18} cm^{-3} ceiling have been made by using co-implantation of Si and As. The result of this work, carried out mainly at Caltech, are reported in Sec. 2.2. The results indicate no increase in the upper limit of free carrier concentration. This conclusion seems to indicate that the threshold is not a function of compensating species, but rather an intrinsic property of Si in GaAs.

2.1 Reproducibility of FET Channel Implants

The control and reproducibility of the electrical characteristics of the FET channel implant are critical concerns for high yield fabrication of IC's. The channel (n^-) implant determines the threshold voltage for switching of the logic gates, and this voltage must be tightly controlled particularly for low voltage, low power IC's.

The technological development and investigation of the n^- implants has been an ongoing activity. Significant progress has been achieved, and it is now possible to report that for a statistically significant period of time, reproducibility has been satisfactory for high yield fabrication of high speed low power SDFL circuits. This result is evident in the data of Fig. 2.1-1, which show the distributions of pinchoff voltage obtained on all the wafers processed throughout a period of over 6 months. The results were obtained by automated probing of 1 μm gate FETs distributed across the processed wafers. A histogram (Fig. 2.1-1) was made for the average pinchoff voltages obtained from each wafer. The overall average pinchoff voltage was 1.12V (as desired for low power, high speed depletion MESFET devices), while th andard deviation of V_p in Fig. 2.1-1 was 110 mV, well within the range required for SDFL circuits. The results include 55 consecutively processed wafers, corresponding to 14 lots and 8 different GaAs substrate ingots. Most of the wafers correspond to Bridgman grown substrates (5 ingots), although the recent Rockwell grown LEC substrate materials are also represented (3 ingots). Comparable control over V_p have been obtained for both types of substrates, provided ingot qualification tests are used for material selection, and implant fluences for IC wafer lots are chosen on the basis of test results with similar material. Preliminary results indicate that on the basis of a fixed implant dose, unselected ingot process, the LEC materials display significantly better reproducibility.

Data on uniformity of V_p across the wafers have similarly been good over an extended time. For the same 6 month period, the median standard

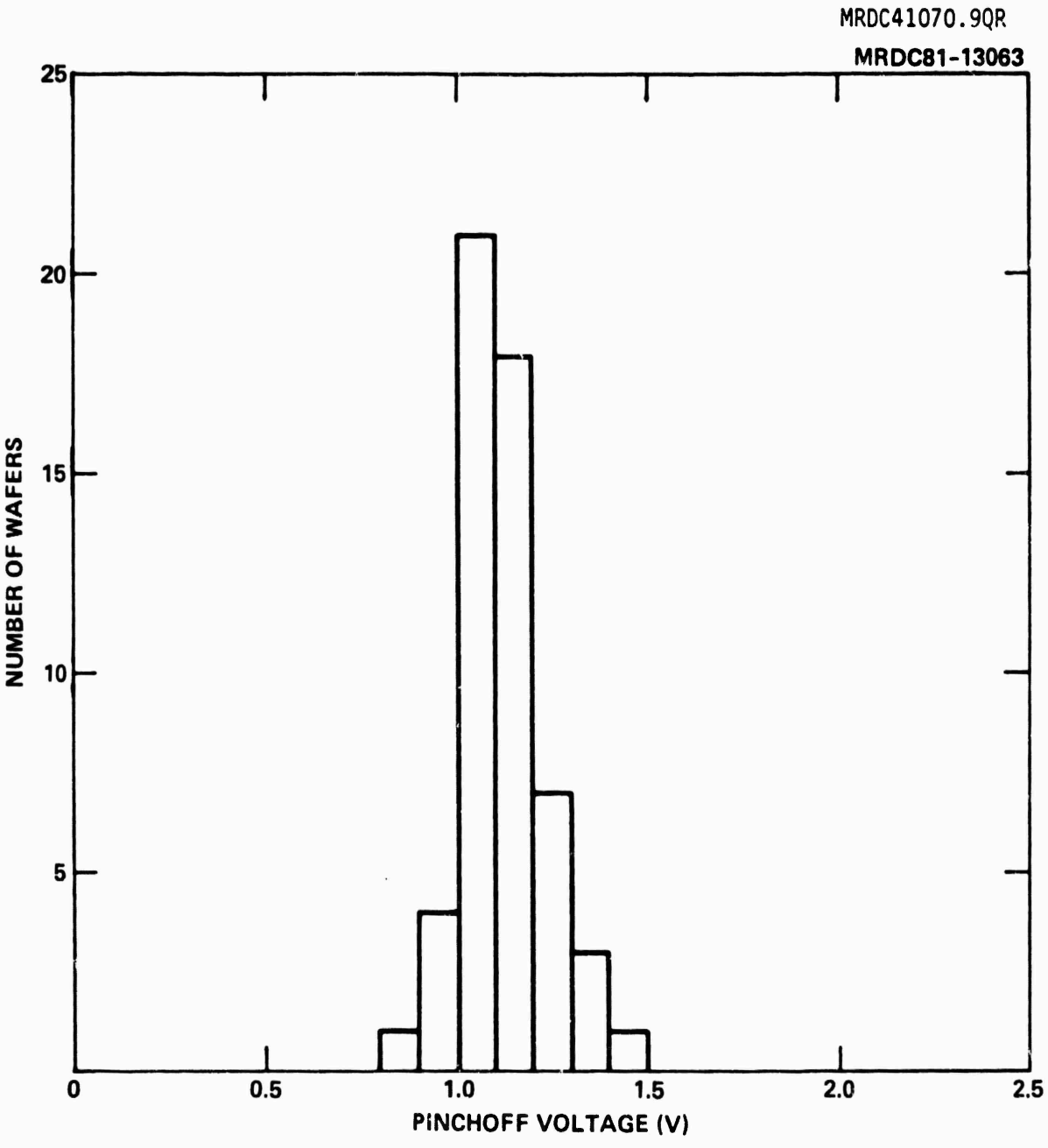

Fig. 2.1-1 Distribution of FET pinchoff-voltage observed in 55 consecutively processed wafers over a 6 month period.

deviation of V_p across the wafers has been only 64 mV. The uniformity of the LEC grown substrates has been significantly better (median standard deviation of V_p of 55 mV) than that for Bridgman substrates (median standard deviation of 84 mV). The superior uniformity is expected on the basis of the improved purity of the LEC material, as well as its growth size and geometry which are better adapted to decrease the effects of impurity segregation during crystal growth.

Sources of variation of V_p among the runs include both process-related and substrate-related effects. As technological improvements are made, variations of V_p on successively finer scales can be extracted from the noise, and the effects of numerous parameters on V_p can be deduced. Recently the effects of implant energy and Si_3N_4 thickness (before and after implantation) have been studied. As shown in Fig. 2.1-2, V_p varies linearly with Se ion energy at approximately 10 mV/KeV. This result is in good accord with the expected result, considering the effect of ion energy on channel depth. If a change in Se implant energy leads to a shift in depth δx of each donor in the channel, then the expected change of V_p with energy is

$$\frac{\delta V_p}{\delta E} = \frac{\delta V_p}{\delta x}\frac{\delta x}{\delta E} = \frac{q}{\epsilon}\phi_{implant}\frac{\delta x}{\delta E} \qquad (1)$$

Here $\phi_{implant}$ is the total implant dose and $\delta x/\delta E$ is the total stopping power of GaAs for Se ions. Using $\phi_{implant} = 2.3 \times 10^{12}$ cm^{-2} and a stopping power of 3.45A/KeV as given by Gibbons et al,[1] the predicted change is 11.4 mV/KeV, in

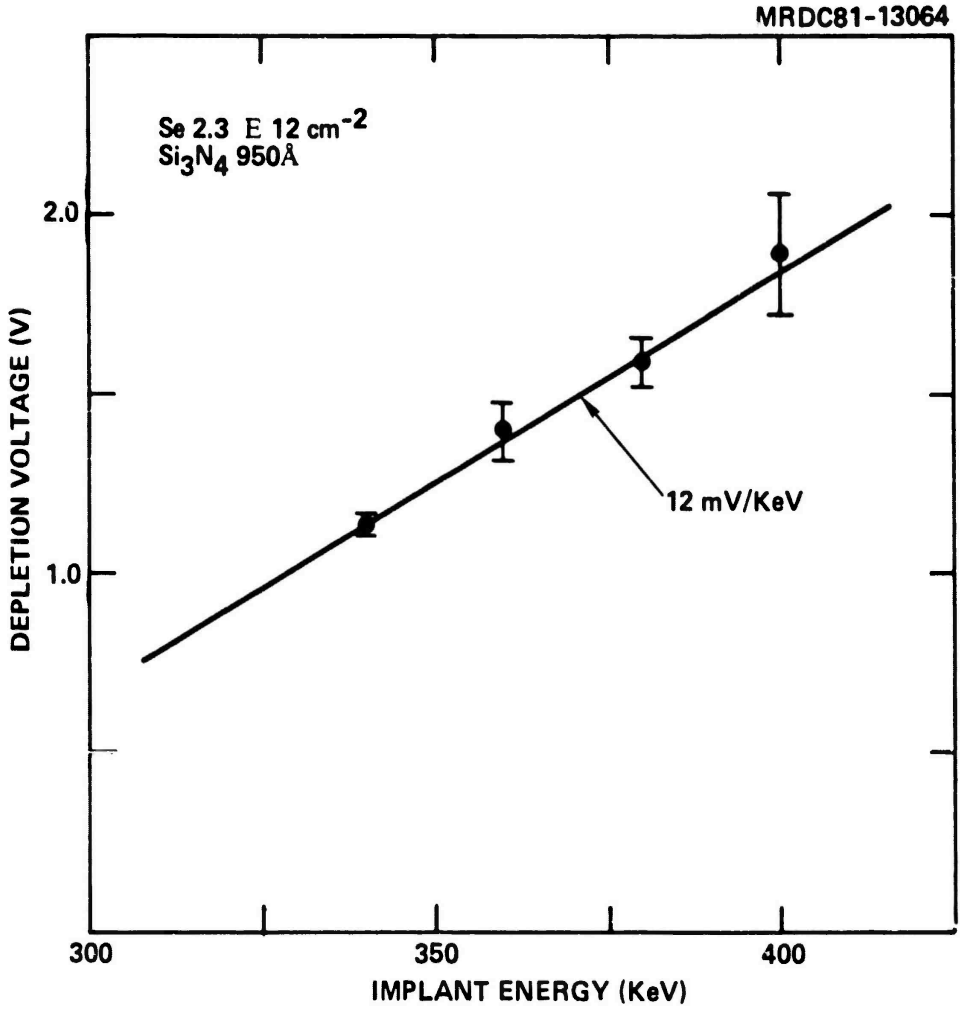

Fig. 2.1-2 Dependence of depletion voltage of Se channel implants on implant energy.

good agreement with experiment. A similar effect is expected for variations in Si_3N_4 cap thickness since in the Rockwell process the cap is deposited prior to implantation. If the stopping powers of Si_3N_4 and GaAs are considered to be equal, then the predicted change of V_p with cap thickness is 3.3 mV/A. This result is again in good accord with experiment, (approximately 3 mV/A) as shown in Fig. 2.1-3.

The stress produced by the Si_3N_4 cap has been a subject of concern for some time. However, recent measurements indicate that changes in cap stress do not cause variations in V_p. This result is inherent in the above results where the cap thickness was varied prior to implantation, since the stress imparted to the GaAs surface is directly proportional to cap thickness. To examine this effect further, a series of samples were capped and implanted, and then the cap was thinned substantially (after implantation). As shown in Fig. 2.1-4, the measured V_p for these samples was constant, even though the cap-induced stress varied by up to factor of 3.

2.2 Dual Implantation of Si and As

Room temperature implanted Si is an excellent n-type dopant in GaAs, generally producing a high degree of electrical activation for low-dose implants.[2] However, an upper 2×10^{18} cm^{-3} limit apparently exists on the achievable free electron concentration, attributed to the formation of neutral Si-Si pairs,[3] fixing the concentration for high-dose implantation. A series of experiments exploring the potential advantages of dual implantation with a complementary ion to enhance the Si electrical activation by maintaining local

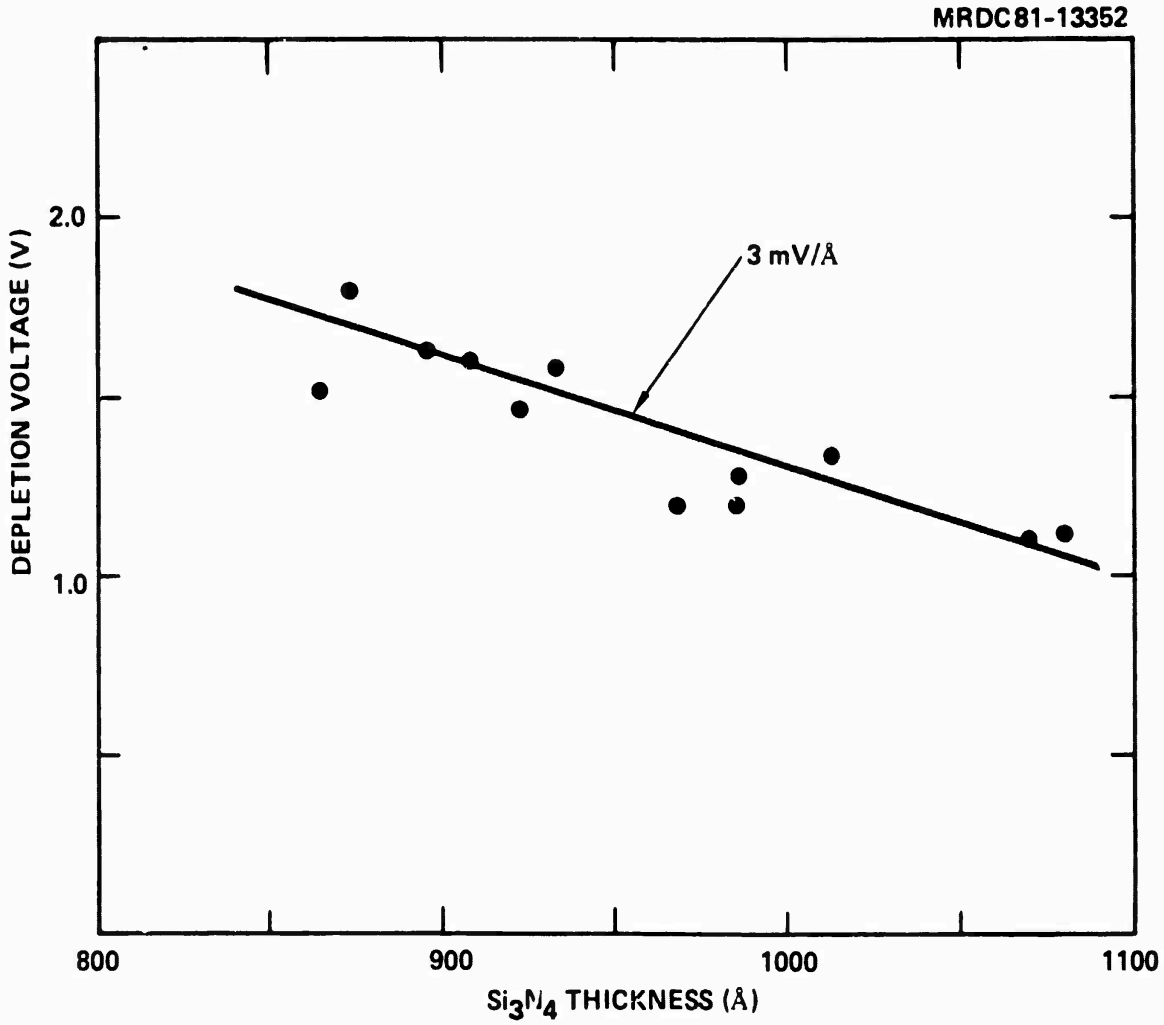

Fig. 2.1-3 Dependence of depletion voltage of Se channel implants on Si_3N_4 thickness prior to implantation.

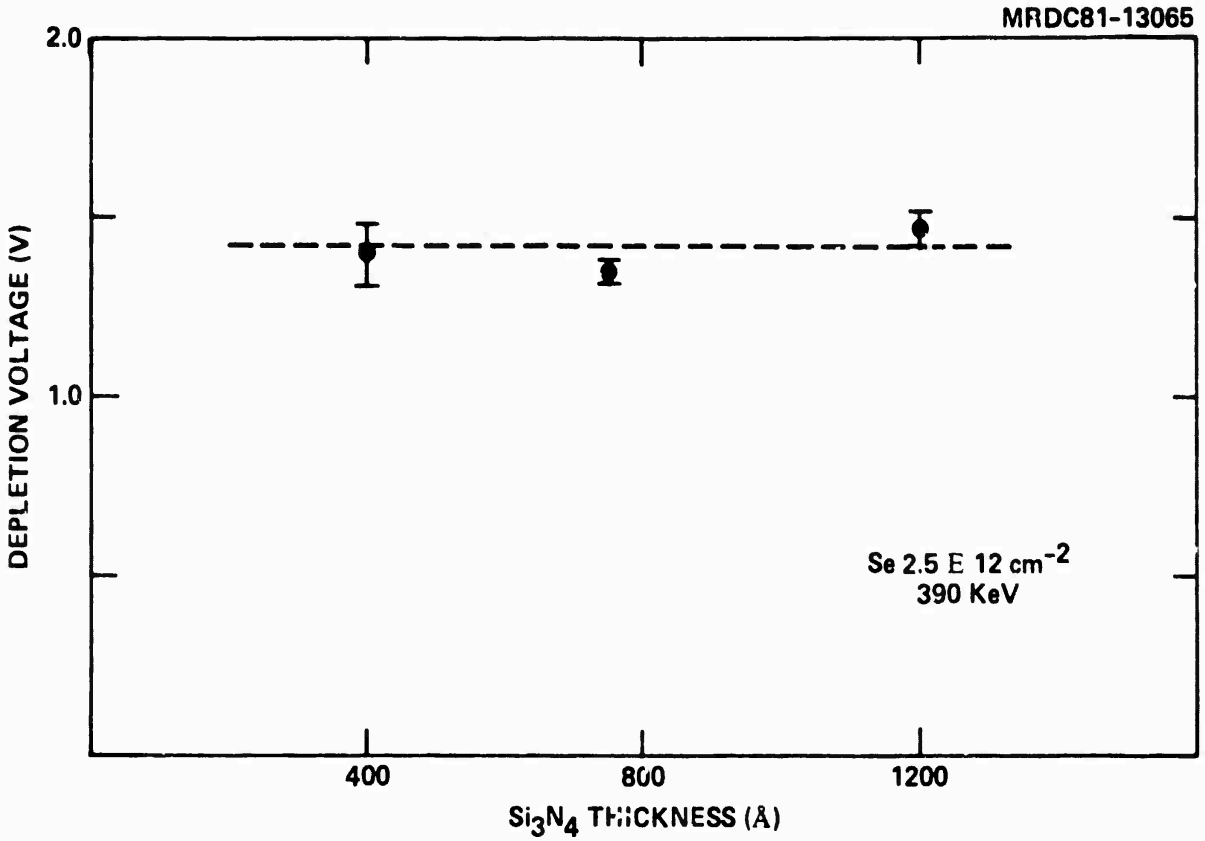

Fig. 2.1-4 Dependence of depletion voltage of Se channel implants on Si_3N_4 thickness during anneal (for constant Si_3N_4 thickness prior to implantation).

stoichiometric balance has been carried out in close cooperation with the Caltech group. These experiments have been completed and in summary, the results indicate that no increase in the upper limit of free carrier concentration was observed, though a given level of activation was achieved at reduced annealing temperatures.

Semi-insulating <100> Cr doped GaAs was implanted at room temperature with 150 keV Si to doses of 10^{13}, 10^{14} or 10^{15} ions/cm^2. Room temperature co-implantations of 360 keV As were also made to doses either five times less, equal to, or five times greater than the primary Si dose. The implanted samples were encapsulated with 2000 A of reactively sputtered Si_3N_4 and annealed at 850 or 900°C for 30 min in flowing hydrogen. All implanted and annealed samples were characterized by sheet electrical measurements using a conventional van der Pauw method. A standard anodic stripping technique was employed for depth profiling of selected samples.[4]

Results of the sheet Hall measurements are presented in Figs. 2.2-1a and 2.2-1b showing sheet electron concentration versus Si dose for annealing at 900 and 850°C. The solid line serves as a reference corresponding to 100% activation. There is 70% electrical activation obtained with the 10^{13} cm^{-2} Si dose, independent of annealing temperature or co-implanted As dose. Samples implanted to 10^{15} Si cm^{-2} show limited activation attributed to Si-pairing, with only a slight enhancement from the co-implanted As. There is incomplete annealing at 850°C as indicated by the twofold increase in electrical activation at 900°C. In contrast to the 10^{13} and 10^{15} Si cm^{-2} cases, there is a discernible effect of As on the electrical activity at 10^{14} Si cm^{-2} with 850°C

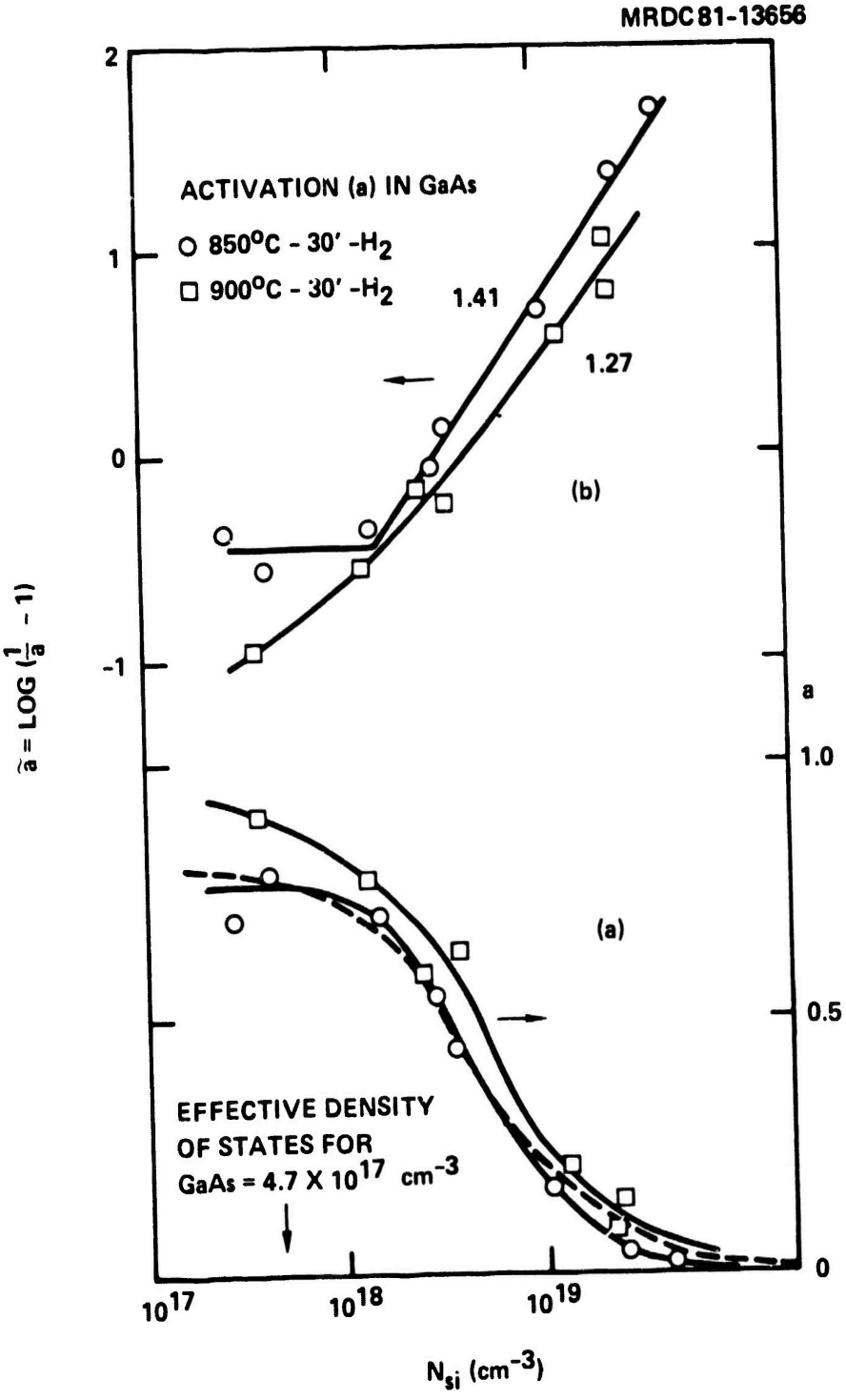

Fig. 2.2-1 Graph of S: Activation in GaAs:
●850°C . 30 min. - H_2
+900°C - 30 min. - H_2

annealing. This effect diminishes at 900°C though the peak sheet concentration does not significantly increase. At both 850 and 900°C annealing, there is ~ 50% electrical activation with 10^{14} Si cm^{-2} in the absence of As.

An additional As implantation initially decreases the sheet carrier concentration with increasing As dose. There is a small increase in activity between the 10^{14} and $5x10^{14}$ As cm^{-2} coimplanted samples.

Figure 2.2-2 shows the sheet Hall mobility verses Si dose for each annealing temperature. The mobility displays the same behavior generally observed for single Si implantations. The increased dispersion in mobility at 850°C relative to 900°C is probably due to incomplete annealing at the lower temperature.

Free electron concentration and mobility profiles for samples coimplanted with 10^{15} Si cm^{-2} and annealed at 900°C are shown in Fig. 2.2-3. The Si and equal-dose As profiles calculated using LSS range parameters in the Edgeworth approximation are also shown.[1] The free electron profiles are essentially constant at 1.6×10^{18} cm^{-3}, independent of As coimplantation. Dispersion in the profiles is within expected experimental uncertainties. The integrated concentrations agree within 25% of the measured sheet values. Coimplanted As has a negligible effect on the mobility profile. It is inferred from the close correlation of these profiles with surface measurements and previously published results[2] that the substrates, the sample preparation, and the measurement techniques employed are reproducible.

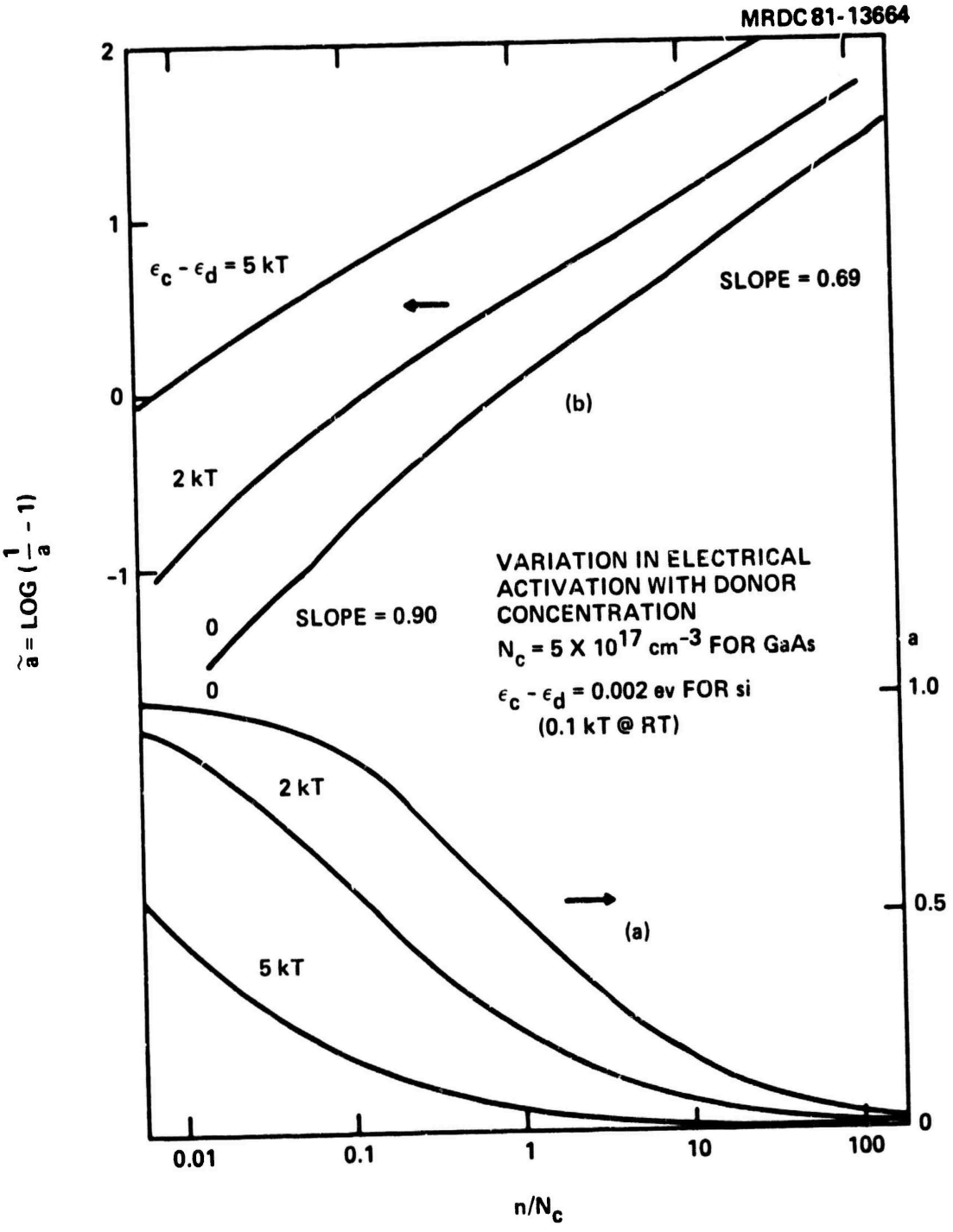

Fig. 2.2-2 Model of donor freeze-out for a shallow donor. Graph of variation in electrical activation with donor concentration.

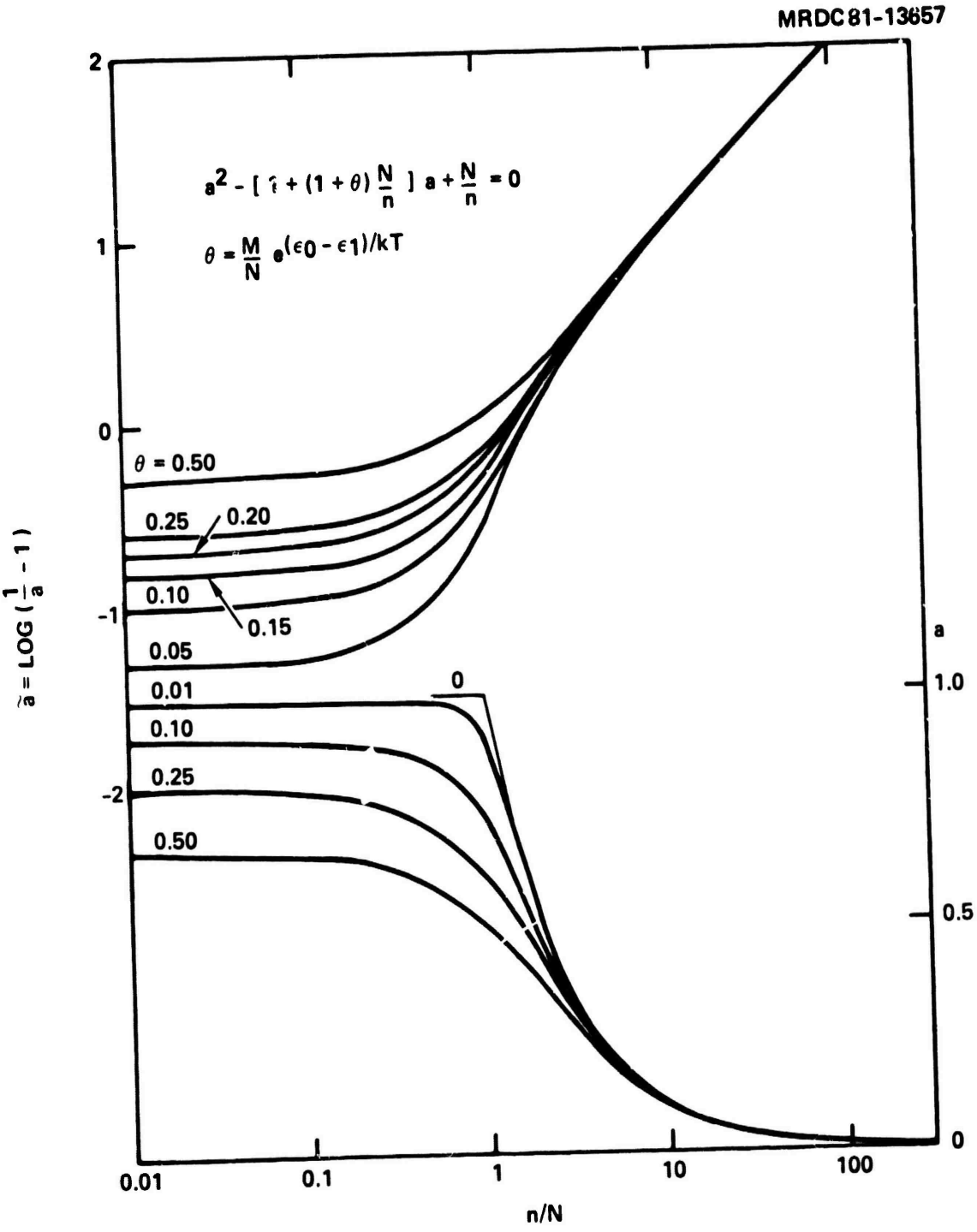

Fig. 2.2-3 Model of saturation with competing process.

The effect of coimplanted As on the free electron concentration and mobility profiles for samples implanted with 10^{14} Si cm^{-2} and annealed at 850°C is shown in Fig. 2.2-4. LSS profiles for the Si and equal-dose As implantations are drawn for comparison. Arsenic has the pronounced effect on the free electron concentration indicated by the surface measurements of Fig. 2.2-1. The limitation of the free electron concentration at ~ 10^{18} cm^{-3} is evident in samples with little or no As. The difference in the two profiles should be considered insignificant and within experimental uncertainty. The integrated concentrations agree within 30% of the corresponding sheet values. An equal implantation of As at 10^{14} cm^{-2} reduces the free electron concentration near the surface by a factor of 25, and produces a large depth dependence. The mobility, in this case, shows the same inverse correlation with the free carrier concentration as is observed in bulk GaAs. With a large As dose, the free electron concentration reaches the saturation level though there is a step at approximately R_p of the LSS profile. The relative uncertainty of the points in the high As dose profile is less than 25% for the first 2400 Å from the surface.

Discussion

It is evident that enhanced Si substitutionality cannot be induced by altering the local stoichiometry with coimplanted As at room temperature. This result indicates that the threshold is not a function of compensating species, but rather an intrinsic property of Si in GaAs.

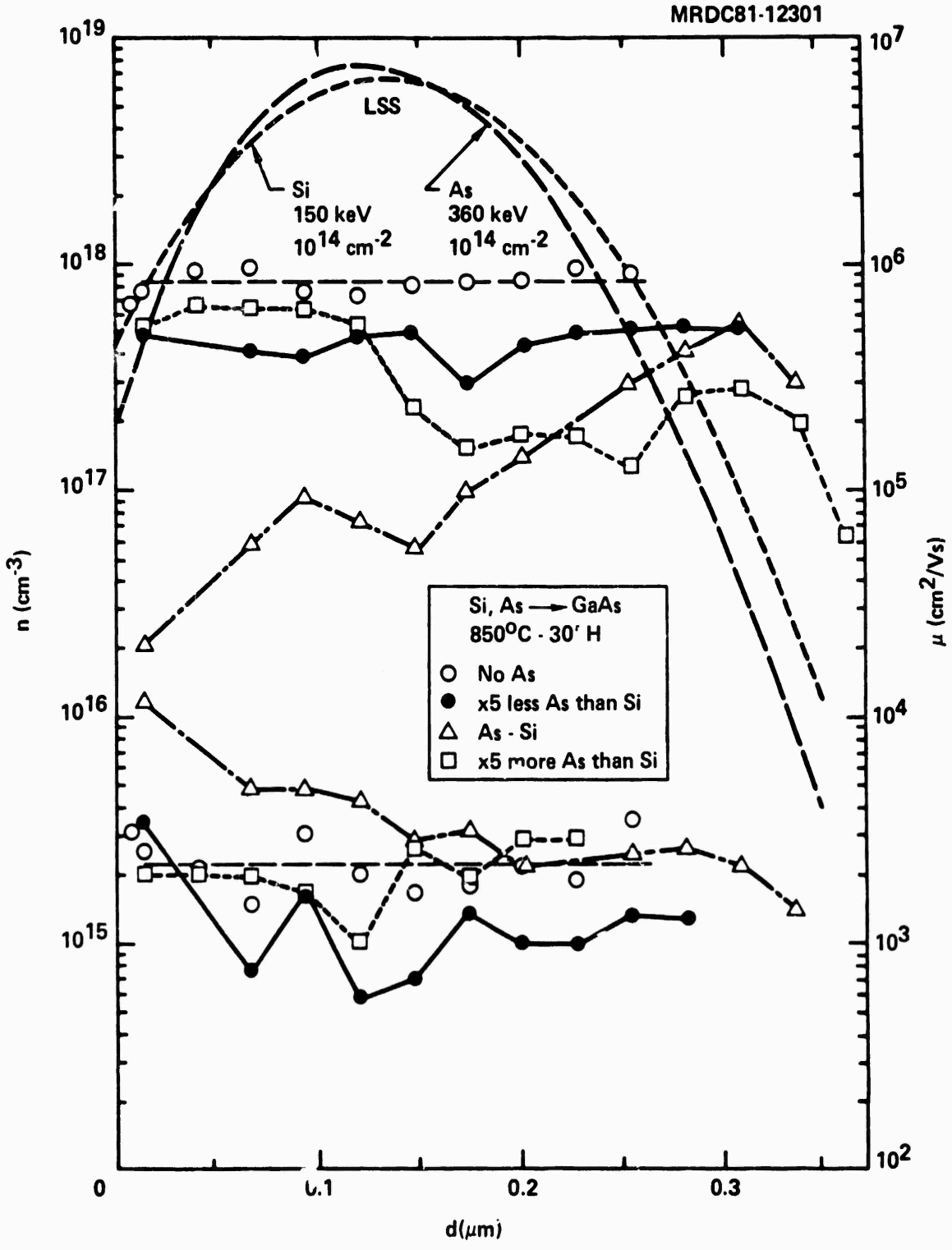

Fig. 2.2-4 Free carrier concentration and mobility profiles for GaAs.

Silicon diffusion is not an important parameter in this investigation either. The profiles for single Si implantation extend to ~ 3.6 R_p for 10^{15} Si/cm^{-2} with 900°C annealing and to ~ 2.5 R_p for 10^{14} Si/cm^{-2} with 850°C annealing. It is evident from the corresponding profiles in Figs. 2.2-3 and 2.2-4 that As does not significantly influence Si redistribution during annealing at 850-900°C.

The morphology of GaAs preceding annealing does not appear to be a factor restricting enhanced substitutionality. Extrapolation of results for the amorphization of GaAs by implanted Si, as established by Grimaldi et al using channeling,[5] indicate that GaAs is fully amorphous to a depth of ~ 2 R_p after room temperature implantation of 10^{15} Si/cm^{-2}. The subsequent As implantation into the amorphized layer is thought to merely extend the amorphous region. In previous work it was shown for single specie implantation that regrowth is primarily governed by the initial amorphous thickness, irrespective of ion specie or dose. It therefore seems likely that the residual damage is qualitatively the same for all samples coimplanted with 10^{15} Si/cm^{-2}. Thus, regrowth of GaAs from the amorphous state is not a sufficient condition at high doses for As to enhance Si activation. In contrast, the implantation of 10^{13} cm^{-2} 150 keV Si leaves the GaAs polycrystalline. Extrapolation of results for the amorphization of GaAs by implanted As indicates that an amorphous layer may have been produced by implanting 10^{13} or 5×10^{13} cm^{-2} 360 keV As, though good regrowth is expected upon annealing because the amorphous layer would have had to be thin (< 500 A). There was certainly no amorphous layer after a 0.2×10^{13} 360 keV As

implantation. It is therefore apparent that to maintain a crystalline structure is not a sufficient condition for enhanced activation with As, either.

The electrical profiles for 10^{14} Si/cm^{-2} (Fig. 2.2-4) suggest that substrate morphology is a factor governing Si activation. In contrast to the behavior shown for 10^{13} and 10^{15} Si/cm^{-2}, coimplanted As has a strong influence on the Si activity at 10^{14} cm^{-2}. Note that this dose coincides with the transition region between the formation of a damaged single crystalline layer and the full amorphization of GaAs by room temperature implantation of Ar, As, S or Si in the energy range of hundreds of keV. The As dose dependence observed in Fig. 2.2-4 most probably arises from an explicit dependence of the residual damage on the As dose in that transition region. The pronounced decrease in free electron concentration at the surface with 10^{14} As/cm^{-2} implantation is probably due to incomplete annealing. The sheet measurements (Fig. 2.2-1) show that the effect of As is less pronounced at 900°C than at 850°C. This further substantiates the conclusion that the effects seen in Fig. 2.2-4 are structural in origin. Since compensation by Cr gettering at the surface is not observed at other doses, Cr compensation is not a likely cause here either. Extrapolation of amorphization ranges reported for As in GaAs indicate that at 5×10^{14} cm^{-2} 360 keV As will produce a fully amporphous region extending to 1-2 R_p. The recovery of the free electron concentration observed with 5×10^{14} cm^{-2} As implantation could therefore be attributed to regrowth from the amorphous state. Whatever the actual causes may be, it is evident that a rigorous characterization of the annealed layer in this

transition region would require careful structural investigation of each particular case.

In conclusion, no indication has been found that Si substitutionality in GaAs can be enhanced by complementary dual implantations at room temperature. The $2x10^{18}$ cm^{-3} free electron limit for Si in GaAs does not appear to be associated with local stoichiometry or regrowth conditions. Coimplanted As does not have a perceptible effect on Si activation except in the transition region of ~ 10^{14} Si/cm^{-2}, where a complete annealing is delayed and a complex behavior is observed.

3.0 PROCESS STABILIZATION

Process stabilization activities focused on improving our LSI process capability have continued during this reporting period. Experiments started during the last quarter, designed to evaluate the advantages of a third n^{++} implant step, have resulted in speed improvement on ring oscillators. This performance improvement is attributed mainly to the lowering of FET source resistance, with comparatively larger speed improvements observed in very low pinch-off voltage circuits. A discussion of this work is presented in Sec. 3.1.

The main yield limiting factor on the 8x8 multiplier LSI circuit has been observed to be shorts between the power supply lines. A statistical evaluation of this problem indicates that random defects creating shorts between adjacent second level metal interconnect lines is the major obstacle. Section 3.2 summarizes our evaluation of this problem, and contains discussion of various process alternatives and planned experiments for improving the metalization lithography yield.

Section 3.3 contains a discussion of our continued work or characterizing and improving the reliability of GaAs ohmic contacts. In Sec. 3.4 initial reliability experiments on integrated circuits are described. A packaged ÷ 80/82 MSI circuit has been tested successfully under bias at 125°C in air for 1700 hours.

3.1 Enhanced Ohmic Contact Development

Completion of the experiment on a third, n^{++}, implant discussed in the last quarterly report[6] has shown correlation between switching speed and doping density under ohmic contact regions. Nine-stage ring oscillators were fabricated on a wafer that was partitioned in four quarters, with each quarter of the wafer receiving separate n^{++} Si implantation doses.[6] The data presented in Table 3.1-1 represent a summary of ring oscillator performance for these four different areas. It can be seen that the frequency of operation increases when the sheet resistance is decreased. A range of ρ from 57 to 453 $\Omega/\square$ results in maximum oscillation frequencies of 360 MHz (τ = 154 ps) and 255 MHz (τ = 218 ps), respectively. The overall ring oscillation speeds are very modest due to the exceptionally low pinch-off voltage MESFETs used in this experiment. However, propagation delays in the 150-200 ps region are quite good considering the associated low power dissipation, providing speed-power products of 24-27 fJ. The scaling of propagation delay with n^{++} doping level will more strongly dominate in a circuit employing low threshold MESFETs circuit (~ 0.6V) like the one tested, as opposed to the more typical, ~ 1.0 V, MESFETs thresholds used for SDFL. This is because reducing source resistance is comparatively more important in MESFET devices with higher channel sheet resistances. Additional experiments will be conducted in order to further verify the impact on speed and the relative overall advantage of the additional doping under the FET ohmic contacts.

Table 3.1-1

Ring Oscillator Performance vs
Sheet Resistance in the Ohmic Contact Region

Wafer Location	ρ_s(Ω/□)	*f(MHz)	τ(ps)	P(μW)	**Pτ(fJ)
Q3	453	255	217.8	123	26.8
Q2	76	295	188.3	127.4	24
Q4	60	302	183.9	141.6	26
Q1	57	360	154.3	171.4	26.4

*Ring oscillators biased for maximum operating frequency.

**The very low speed power products are a result of having very low threshold voltages (V_p = 0.577 V) on the 10 μm wide MESFETs.

3.2 Multi-level Interconnect Yield

Analysis of the 8 x 8 multiplier (1008 gates) results has indicated that one of the main problems limiting the functional yield of these circuits is the appearance of electrical shorts between power supply lines. Out of a total of 960 multipliers tested, 599 (62%) were found to have shorted power supply lines. Assuming that this problem is not associated with shorts in the active devices, or isolation failures, it must be attributed either to failure of crossover of second over first level metal, or to shorts between two adjacent power supply lines (SDFL power supply lines are mainly designed as part of the second-level interconnects). As described in previous reports,[6] the planar crossover techniques used in this work have, inherently, very high yield. Recent evaluation has verified this premise. A large number of crossover test structures containing 9,000 crossovers per structure, evaluated on 6 randomly chosen wafers yielded 86% (248/288) fully functional structures with a ±8V test voltage applied between first and second level metal interconnects. This is a good result considering that every structure on each wafer was measured, and no effort was made to pre-screen wafers that were thought to have better lithographic yield. Furthermore, at least one wafer exhibited 100% yield corresponding to 432,000 isolated crossover structures on that wafer.

Without any other indication to the contrary, it appears that shorts between adjacent second-level metal power supply lines are responsible to a large degree for the limited yield observed on the 8 x 8 multipliers. It should be clarified that this is a first order lithography yield limitation,

which must be improved before additional device and circuit yield analysis can be performed. Good yield on the second level interconnects is a necessary, but not sufficient condition for successful operation of these LSI chips.

Electrical Test vs Visual Inspection

The overall test results of the 8 x 8 multipliers showed that 62% of the circuits suffered from shorts. Therefore, a thorough visual inspection of every 8 x 8 multiplier die on 5 wafers was conducted. Figure 3.2-1 shows the three typical second level interconnect defects found on these wafers, which all can lead to shorting between adjacent metal lines. The three major defects are: nonuniformity of metal thickness (evaporation splattering); photoresist residue; and random dust or particles. Table 3.2-1 contains the results of this visual inspection showing the relative percentage of each type of defect. The conclusion from Table 3.2-1 is that second level metal splattering is one of the key problems. Table 3.2-2 contains a summary of visually defective dies for both first (SM) and second level metal (2M) defects. The table shows that the total number of shorted circuits 97/160 (61%) on these 5 wafers is representative and in good agreement with the 62% electrical failures observed for all of the processed 8 x 8 multiplier wafers. As indicated in Table 3.2-2 the largest number of defects (64%) was found on the second level metal, with only 26% of the die showing first level metal defects. A small percentage of the dies, 13%, had simultaneous first and second level metal defects. In summary, the data collected to date indicate

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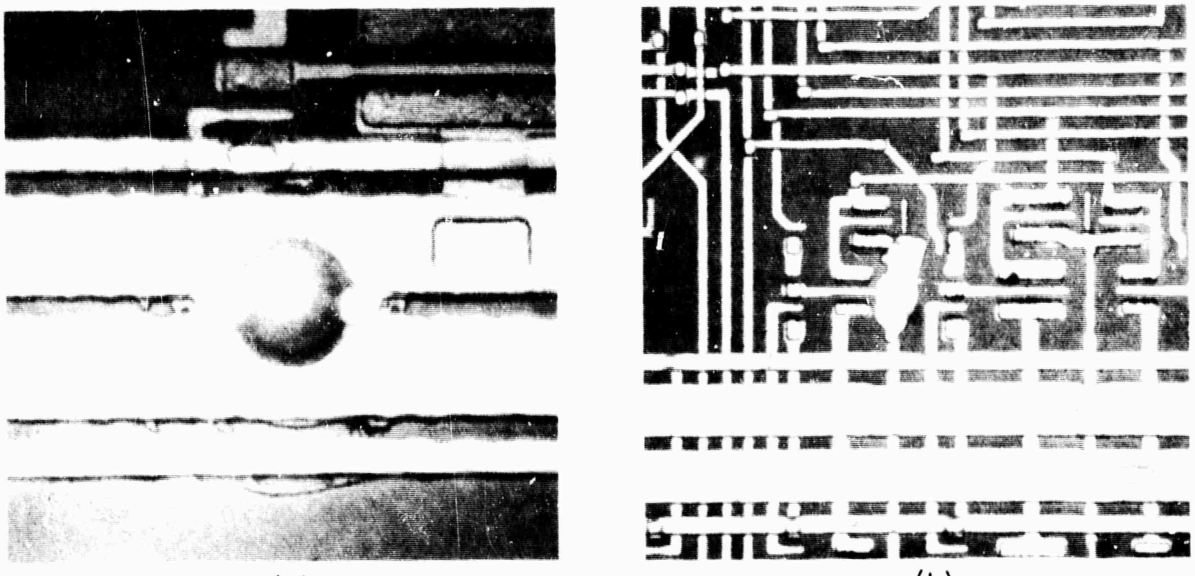
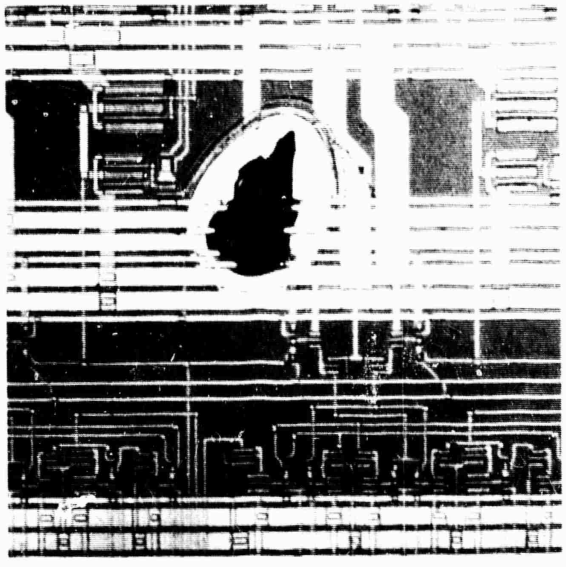


(a) (b)



(c)

Fig. 3.2-1 Photomicrograph of three typical defects causing second level interconnects shorts: (a) nonuniformity of metal thickness, (b) photoresist residue, and (c) dust.

Table 3.?-1

Classification of Second Level Interconnect Defects*

Wafer	TYPE OF DEFECT		
	Metal Splatter	Photoresist Residue	Random Particle
AR5-22	10	12	6
AR5-23	5	10	5
AR5-51	6	12	4
AR5-61	24	6	4
AR5-81	15	2	12
	45% (60/133)	32% (42/133)	23% (31/133)

*Total number of defects observed, eventually more than one per circuit.

Table 3.2-2

Summary of Visual Inspection for First (SM) and Second (2M) Metal Interconnect Defects

ELECTRICAL TEST		VISUAL INSPECTION OF MULTIPLIER CIRCUITS		
Wafer	Shorted Devices/ Total Devices	Number SM Defects	Number 2M Defects**	Number Both 2M, SM
AR5-22	24/32	9	25	4
AR5-23	10/32	11	7	2
AR5-51	11/32	8	17	7
AR5-61	30/32	5	30	4
AR5-81	22/32	8	24	3
	61%(97/160)	26%(41/160)	64%(103/160)	13%(20/160)

*Regardless of 2M defects

**Regardless of SM defects

that the first order defects on the 8 x 8 multiplier circuits are in the second level interconnects.

Discussion

The second level interconnects are defined by ion milling, where energetic ions bombard the surface and sputter atoms from it. Over etching is the method used to insure complete removal of the desired material. However, overetching is not adequate for completely removing all the material from areas where the metal thickness is much greater than the average (splattering), or from areas which have foreign materials such as photoresist residues or dust particles. Incompletely etched metal can result in defective shorted patterns, and it can lead to problems such as shorted power supply lines.

Currently, the second level metalization is deposited by e-beam evaporation. Variations on the deposition method are being studied in order to minimize metal splattering. One approach is to use a large charge with better cooling of the hearth, while another approach is using faster deposition rates. The faster deposition rate approach looks more promising for reducing splattering. Currently a 15 A/s deposition rate is being used. This is superior to the old 7.5 A/min standard. However, improvements in the evaporation do not appear to be totally satisfactory and further changes in deposition methods are planned in the future.

Magnetron sputtering is under evaluation as an alternative deposition technique. Magnetron sputtered films have excellent via step coverage and do

not exhibit any splattering. The magnetron sputtering system used for these experiments is equipped with a planetary fixture allowing films to be deposited with ±3% thickness uniformity. However, this system, with a small (~ 4") target and a large planetary, deposits films of rather high resistivity. Because of the mechanism of the planetary, the substrate is traveling in and out of the deposition zone, allowing Ar atoms to be trapped in the successive layers of deposited material, thereby increasing the resistivity of deposited films. The bulk resistivity of Au films deposited by magnetron sputtering is 0.040 Ω-μm, which is 1.7 times higher than films deposited by e-beam evaporation (0.0235 Ω-μm). To reach the same conductance, the magnetron sputtered Au film thickness must be 1.7 times that of an e-beam evaporated film.

Au films have been deposited on substrates held stationary under the magnetron sputtering target. The resistivity of these films are 0.032 Ω-μm, which is slightly better (80%) than the resistivity that of films deposited with planetary motion as mentioned above. However, the variation of deposited film thickness over a one inch square wafer is rather large (~ 10%). A new magnetron sputtering system which will be compatible with 3" diameter wafers is planned in conjunction with the overall equipment upgrade direct toward large wafer processing. This new capability will provide the desired electrical characteristics, uniformity and splatter free films necessary for the GaAs IC applications.

In addition to splattering of the deposited Au films, photoresist residues and random particles may have also limited the processing yield of

the multipliers. Better processing procedures relating to minimizing processing defects are being implemented where practical. For instance, in the photolithography area a large recirculated, filtered developer bath is being installed in order to minimize photoresist residue. Ionized air guns are being installed in various processing areas. All equipment upgrades will allow wafers to be processed in the vertical or inverted position to minimize the number of particles falling on the wafers.

To evaluate the improvements of second level metal process, a yield test mask set has been fabricated. The mask has two sets of inter-digitated lines which can be electrically tested for shorts between two adjacent lines. A sketch of the test structures is shown in Fig. 3.2-2. The mask set has both light field and dark field versions so that it be can be used both with ion milling and lift-off techniques. A photomicrograph of part of the test structure is shown in Fig. 3-2-3. Pattern A has 3 μm lines with 2 μm spacing, and pattern B has 8 μm lines with 2 μm spacing. The length of each parallel line is 1200 μm. Both patterns A and B have separated test sets which can be independently analyzed. The total length of adjacent lines in a set starts with 12,000 μm and increases by doubling up to 144,000 μm. There are two pairs of pattern A and B in each chip of 2.7 x 2.7 mm; 72 pairs in a 25 x 25 mm wafer. Two mask levels can be used to further check the integrity of crossovers. There are 131,520 crossovers in each chip. This is over 10 times the number of crossovers in the 8 x 8 multiplier (~12,000 crossovers).

Monitoring of improvements in metalization, photolithography, and reduction of particle defects will be made using the test mask described above over a period of time in order to assess progress.

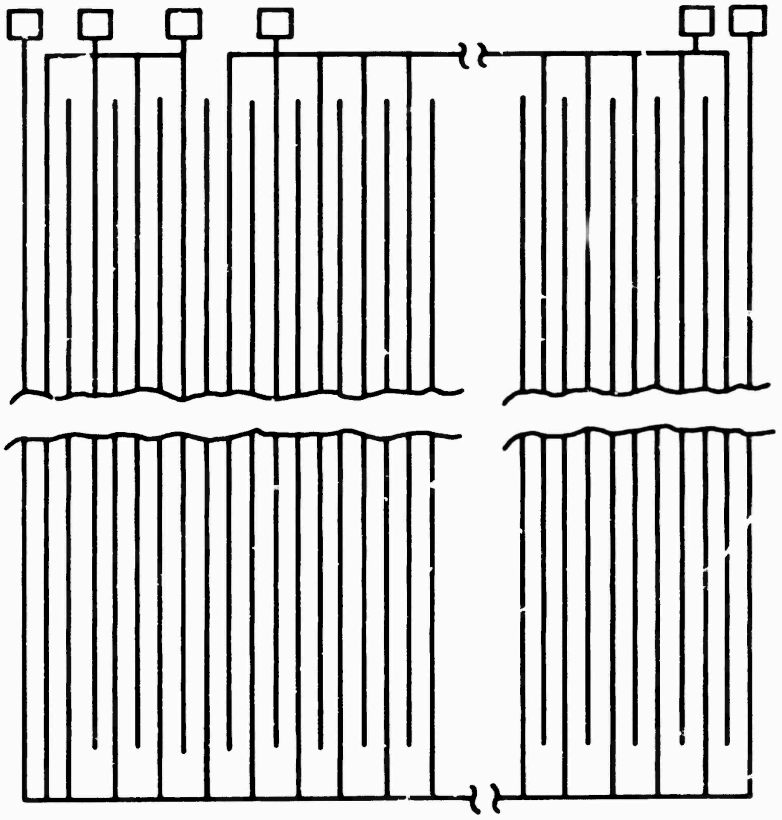
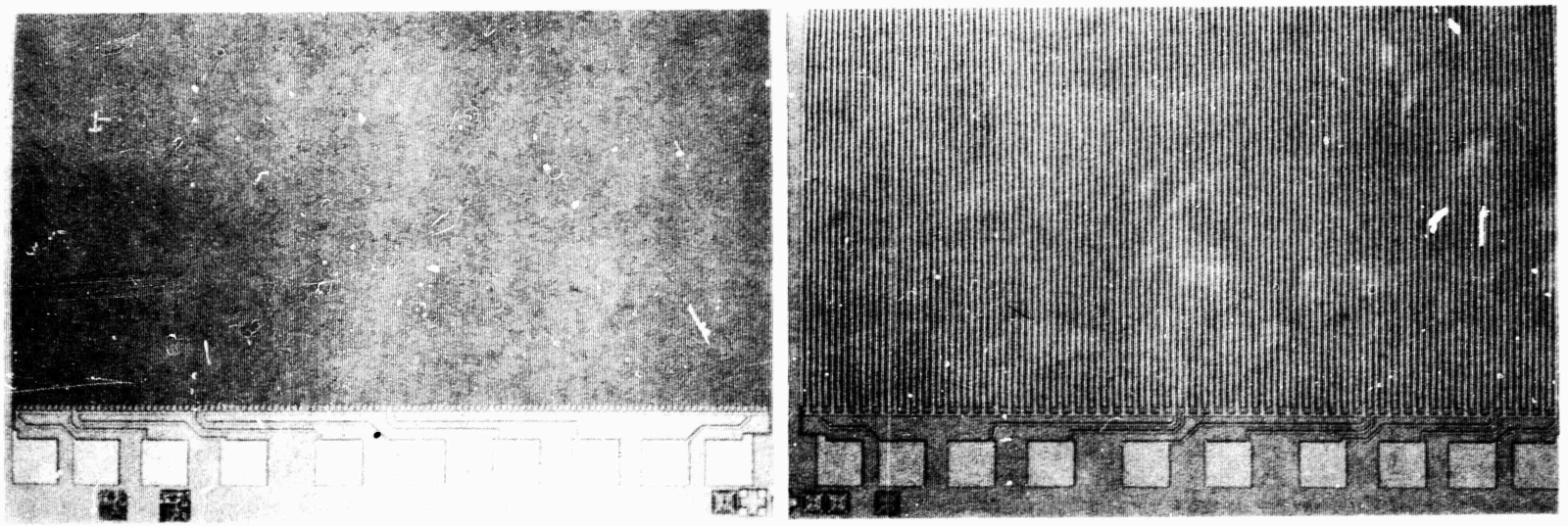


Fig. 3.2-2 Schematic of second level interconnects yield test pattern.



(a) (b)

Fig. 3.2-3 Photomicrograph of part of the second level interconnects yield test structure.

3.3 Ohmic Contact Reliability

The thermal stability of metal contacts to GaAs devices is probably the most important factor in determining the device reliability. It was determined in the previous quarters[6] that between the two metal contacts, ohmic and Schottky used in our IC process, the ohmic contacts are the ones which limit circuit reliability. The deterioration of the ohmic contacts has contributed to the degradation of device characteristics such as the saturation current of FETs and the series resistance of diodes. As indicated in the last report,[6] AuGe/Pt, the ohmic metal which has been used in the past, is not reliable when thermally treated at high temperature (>200°C). Therefore, our standard ohmic metallization system has been changed from AuGe/Pt to AuGe/Ni, which has exhibited a much better thermal stability. During the past months a thorough study of the long-term reliability of AuGe/Pt and AuGe/Ni, and the effect of the overlay metal on reliability has been carried out.

The preparation procedure for the samples used in this study was the same as that of our planar GaAs IC process.[7] An Au-Ge alloy film (88% Au, 12% Ge, ~ 1300 A thick) was evaporated on an n type layer (sheet resistance ≈ 350 Ω/□) formed on semi-insulating GaAs by ion-implantation. The Au-Ge layer was covered by a ~ 300 A thick film of Pt or Ni. Test structures for contact resistance measurements conforming to the transmission line method (TLM)[8] were generated by photolithographic and lift-off techniques. Three different overlay metal schemes were tried. They are Ti/Au (300 A/2700 A), Ti/Pt/Au (300 A/300 A/2400 A) and TiW/Au (500 A, 10% Ti-90% W/2500 Au). The metals were deposited by E-beam evaporation with the exception of TiW which was

deposited by magnetron sputtering. In order to have a fair comparison, AuGe/Pt and AuGe/Ni contacts were fabricated on the same wafer. All of the experimental wafers (1x1 inch) contained 72 TLM ohmic test structures uniformly distributed across the wafers. Wafers containing different overlay metal were fabricated. After overlay metal deposition, the wafers were thermally aged at 250°C in air ambient for reliability test. The specific contact resistance was measured at different stages of aging.

Figure 3.3-1 shows the specific contact resistance vs aging time (at 250°C) for a wafer (wafer A) which had a Ti/Au overlay on half of the wafer. As indicated in the figure, each quadrant of the wafer had a different combination of ohmic and overlay metal. Curves 1 and 2 correspond to AuGe/Pt with and without a Ti/Au overlay respectively; curves 3 and 4 are for AuGe/Ni with and without overlay. The results of the contact resistance measurements on wafer B which had a Ti/Pt/Au overlay, and on wafer C which had a TiW/Au overlay, are shown in Fig. 3.3-2 and Fig. 3.3-3 respectively. Wafer B was divided into four quadrants, the same as wafer A, and wafer C was divided into two halves with different metal combinations.

After ohmic contact alloying and before the overlay metal was put on, both AuGe/Pt and AuGe/Ni were found to be very good contacts with specific contact resistance ranging between low 10^{-6} Ω-cm^2 and high 10^{-7} Ω-cm^2. However, when overlay metals were added on, the AuGe/Pt contacts started to degrade. After a very short (few hours) heat treatment at 250°C, the specific contact resistance raised above 10^{-4} Ω-cm^2. This degradation phenomenon was observed with all three metal schemes. Without overlay, AuGe/Pt is stable even after a

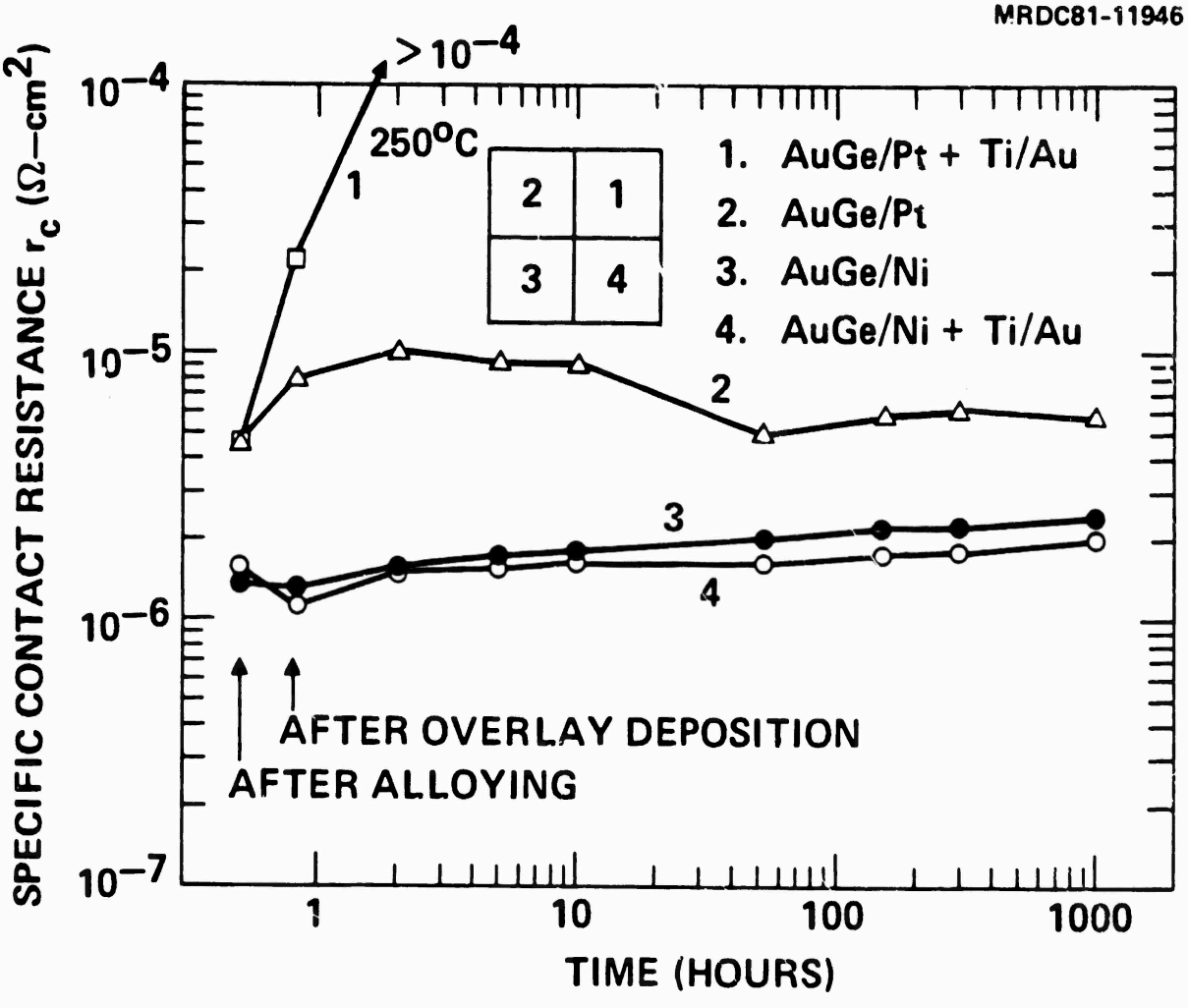


Fig. 3.3-1 Specific contact resistance as a function of thermal aging time (at 250°C), curve 1: AuGe/Pt with Ti/Au overlay; curve 2: AuGe/Pt without overlay; curve 3: AuGe/Ni without overlay; curve 4: AuGe/Ni with Ti/Au overlay.

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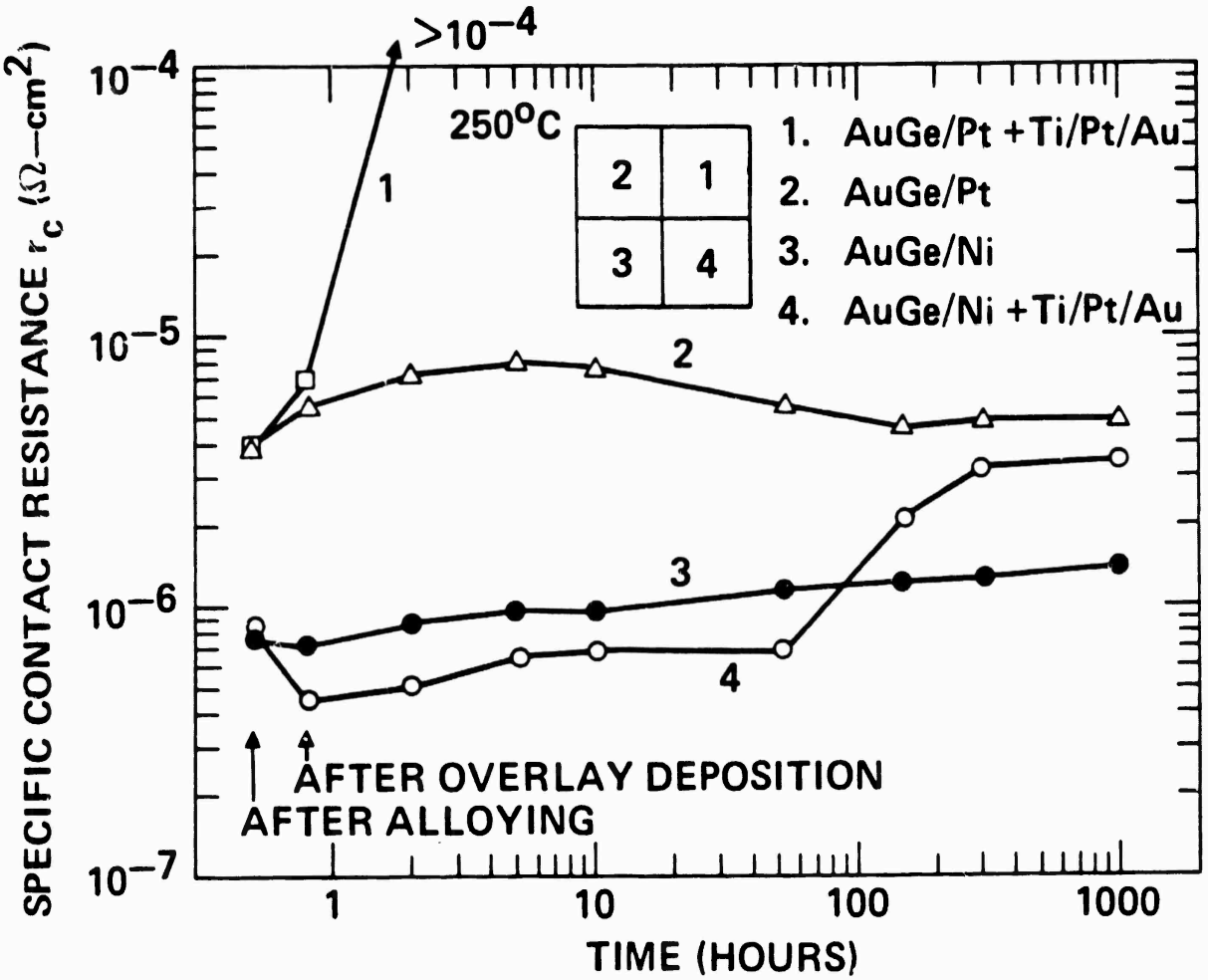

Fig. 3.3-2 Specific contact resistance as a function of thermal aging time (at 250°C), curve: AuGe/Pt with Ti/Pt/Au overlay; curve 2: AuGe/Pt without overlay; curve AuGe/Ni without overlay; curve 4: AuGe/Ni with Ti/Pt/Au overlay.

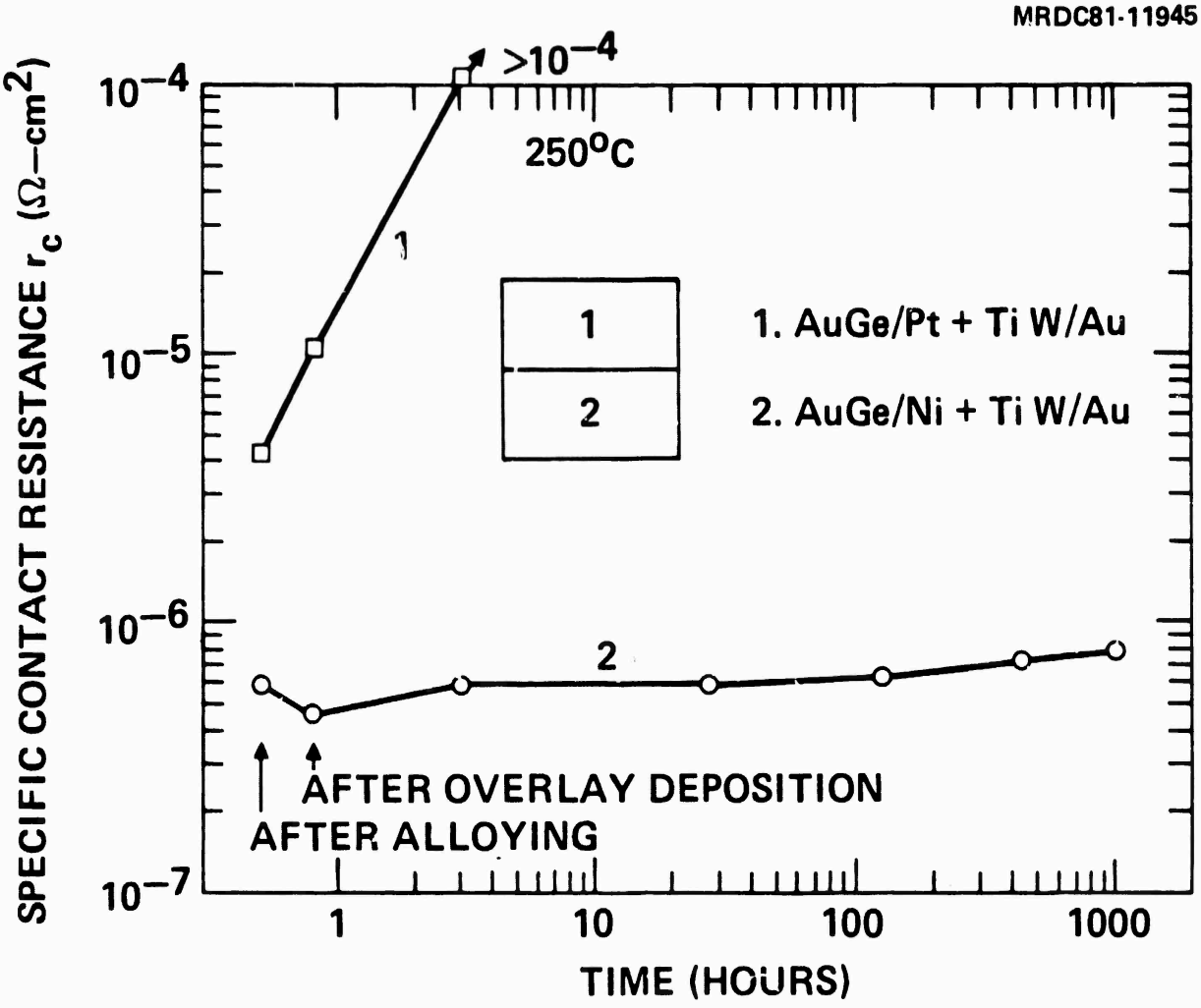

Fig. 3.3-3 Specific contact resistance as a function of thermal aging time (at 250°C); curve 1: AuGe/Pt with TiW/Au overlay; curve 2: AuGe/Ni with TiW/Au overlay.

1000 hour heat treatment. On the other hand, AuGe/Ni contacts show excellent reliability with and without overlay metal. They have lower contact resistance than AuGe/Pt, and the resistance remains low after aging (up to 1000 hours).

Comparing the data presented in the three figures an interesting phenomenon can be seen in Fig. 3.3-2. The specific contact resistance curve (curve 4) of AuGe/Ni with Ti/Pt/Au overlay makes a transition from the 10^{-7} Ω-cm^2 range to the low 10^{-6} Ω-cm^2 range after heat treatment for about 150 hours. The rate of increase of contact resistance lowers after the transition. The curve levels off and approaches the curve of AuGe/Pt (curve 2). This phenomenon, which is only seen with Ti/Pt/Au and not observed with Ti/Au or TiW/Au can be explained as follows: after aging for about 100 hours, the Pt in the overlay diffuses through the Ti layer and reaches the AuGe/Ni region. In AuGe/Ni, it spreads out quickly and forms a compound with Ge.[9] As more Pt diffuses in during the thermal aging process, Pt competes with Ni apparently changing the ohmic contact characteristics from those of AuGe/Ni to those of AuGe/Pt.

The metallurgical mechanism of the rapid degradation of AuGe/Pt when covered with overlay metals is not clearly understood at this stage. The behavior (or movement) of Pt in this metal system is probably influenced by the presence of the additional layer of overlay metal. Since Pt can react with GaAs[10] and is known to form a compound with Ge, this change in behavior could be sufficient to cause the degradation of ohmic contact.

The long term reliability results discussed above confirm the conclusions reached from the short time thermal aging experiments presented in the last report. The decision of changing our standard ohmic contact metal from AuGe/Pt to AuGe/Ni was made at the end of last year. Figure 3.3-4 shows the history of the contact resistance (R_C) and specific contact resistance (r_C) over a recent period of time. These data were obtained through the routine process evaluation measurements taken with our automatic test facility.[11] Each point in the graph represents the average value of R_C or r_C on a wafer. A transition at the end of 1980 resulting in lower contact resistance as a consequence of replacing AuGe/Pt by AuGe/Ni is clearly seen in the figure.

3.4 Circuit Reliability

One ÷80/82 circuit containing 60 gates, packaged in a 16 lead flat pack was tested under bias for a total of 1060 hours at 125°C in air ambient environment.

The table below (Table 3.4-1) shows the bias voltage required to perform the ÷ 82 function with a clock frequency of 800 MHz. Bias voltages and clock input signal were applied throughout the test.

It should be noted that minor bias adjustments (on the order of tens of mV) were required to maintain the ÷82 function and that these adjustments are included in the above table, i.e. the minor changes shown are not entirely due to power supply drift. The ÷80 function was always in a comfortable range

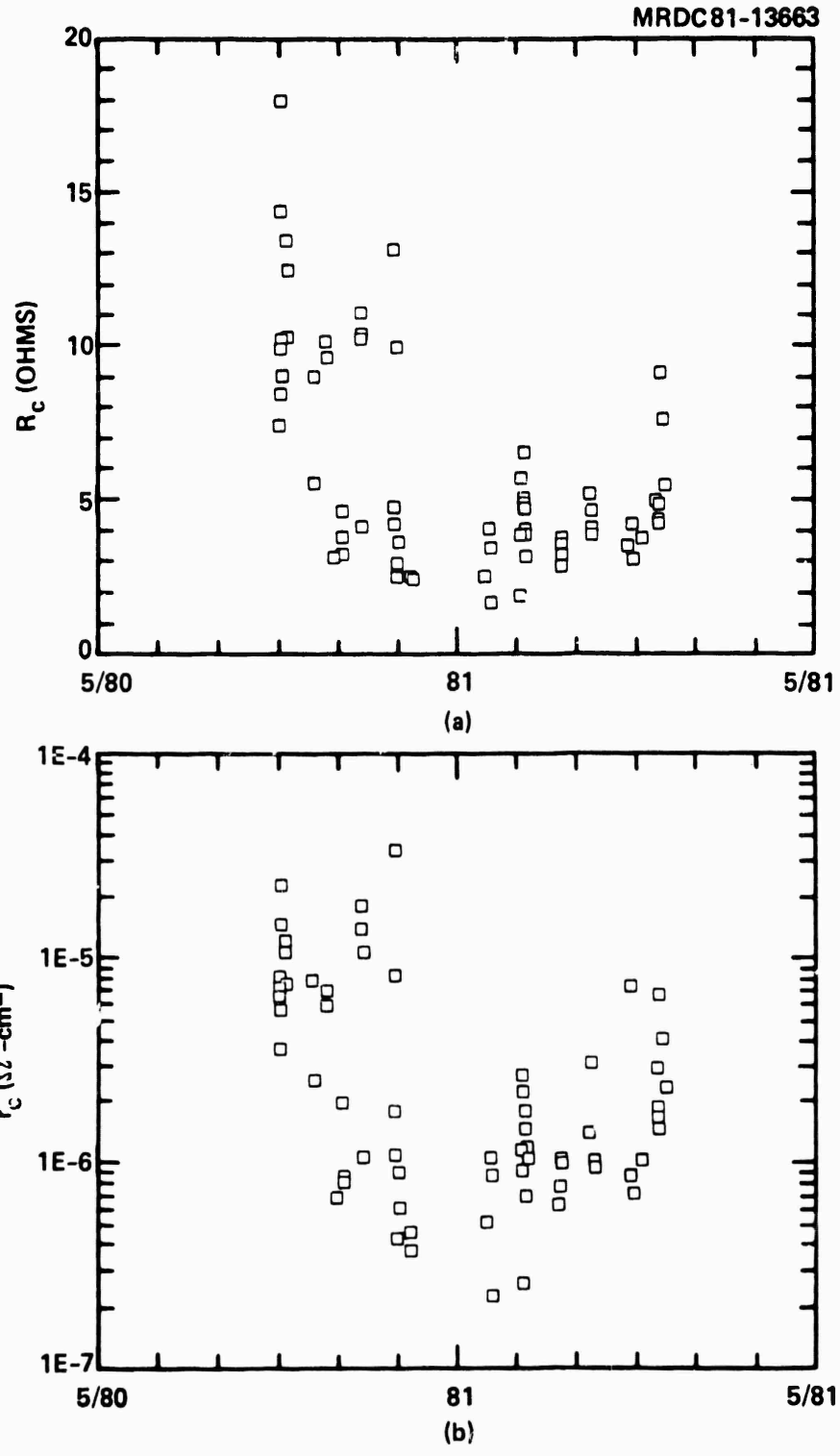

Fig. 3.3-4 History of ohmic contact resistance over a 12 month period. Each data point corresponds to the average for one wafer of (a) total contact resistance and (b) specific contact resistance.

Table 3.4-1

Bias Voltages for Aging Experiments on ÷ 80/82 Circuits

Time (hrs)	V_{DD} (volts)	I_{DD}(mA)	V_{SS}	I_{SS}	V_{pd}
0	3.10	52.4	3.05	16.2	3.46
200	3.0	51.2	3.05	15.9	3.47
400	3.03	51.0	3.05	15.8	3.46
600	3.05	50.8	3.06	15.8	3.47
800	3.06	50.6	3.07	15.9	3.48
1000	3.06	50.7	3.03	16.0	3.42
1400	3.07	50.7	3.08	16.1	3.46
1700	3.18	50.7	3.14	16.3	3.51

of operation. The decrease in the currents I_{DD} and I_{SS} are attributed to changes in the resistance of the ohmic contacts made of AuGe/Pt. New circuits with AuGe/Ni contacts will be tested in the future.

This circuit operated at room temperature at 1 GHz, and had also been subjected to tests at temperatures ranging from -50°C to 125°C prior to this test.

The effect of testing a device at an elevated temperature is equivalent to extending the length of the test at lower temperatures. If the device lifetime versus temperature follows the Arrhenius relation, and the activation

energy is 1 eV (this is conservative as compared to the reported 1 - 2 eV activation energy for discrete GaAs FETs), 1000 hours lifetime at 125°C is equivalent to 4.48×10^3 years at room temperatures. Tests at higher temperatures and/or for longer periods of time are planned for a number of devices to determine the mean time to failure (MTTF) of these devices.

4.0 CIRCUIT DESIGN

All design and digitizing were completed for the AR6 mask set containing the SD^{2}FL 8x8 bit parallel multipler, and the 8-stage and 7-stage code generators. The organization of the mask set is described in Sec. 4.1. Additional design features, incorporated to facilitate obtaining circuit yield data are also discussed. Section 4.2 contains a discussion of the two dimensional numerical calculations carried out at North Carolina State University to model the FET structures used in this program. Preliminary calculations were made using a uniform carrier density profile, and were followed by calculations using a Gaussian profile to simulate an ion implantation profile. Good agreement with experimental data was obtained for the static characteristics, with further improvement expected for a more accurate carrier concentration profile. Work on incorporating a Monte Carlo calculation, and a time dependent (transient) analysis is in progress.

4.1 AR6 Mask Set

During the third quarter, all designs and digitizing were completed for the AR6 mask set, and the mask set was ordered. The mask comprises three reticles; viz., CMD for the SD^{2}FL 8 x 8 multiplier (see Fig. 4.1-1), CDC for the 8-stage and 7-stage code generators (see Fig. 4.1-2), and PCM for process control, and special test circuits (see Fig. 4.1-3). The three reticles are arranged as shown in Fig. 4.1-4, to form the mask which is then stepped 4 times (in a 2 x 2 array) on the wafer. Thus, a wafer has 20 multiplier

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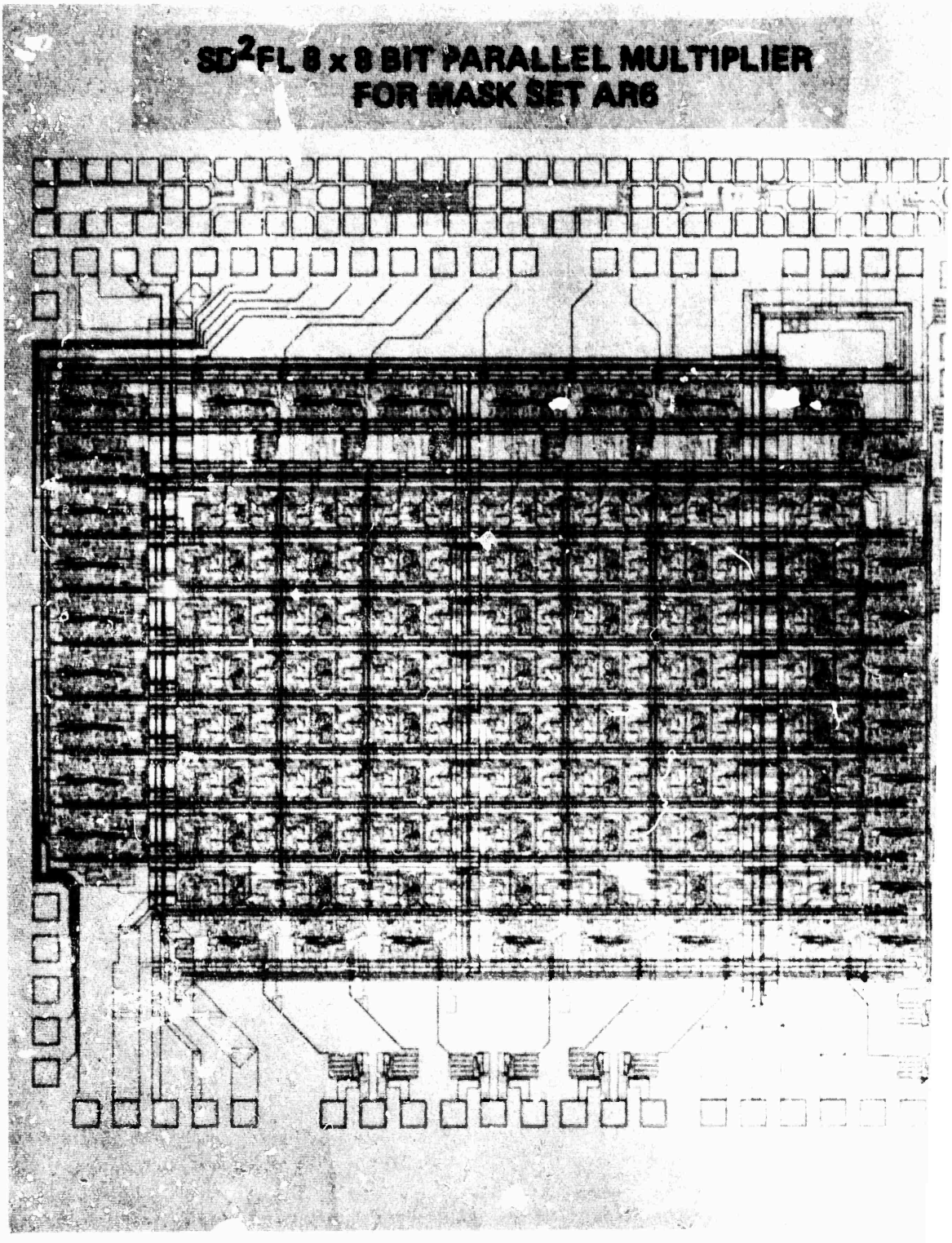


Fig. .1-1 Layout of the SD^{2}FL 8 x 8 multiplier.

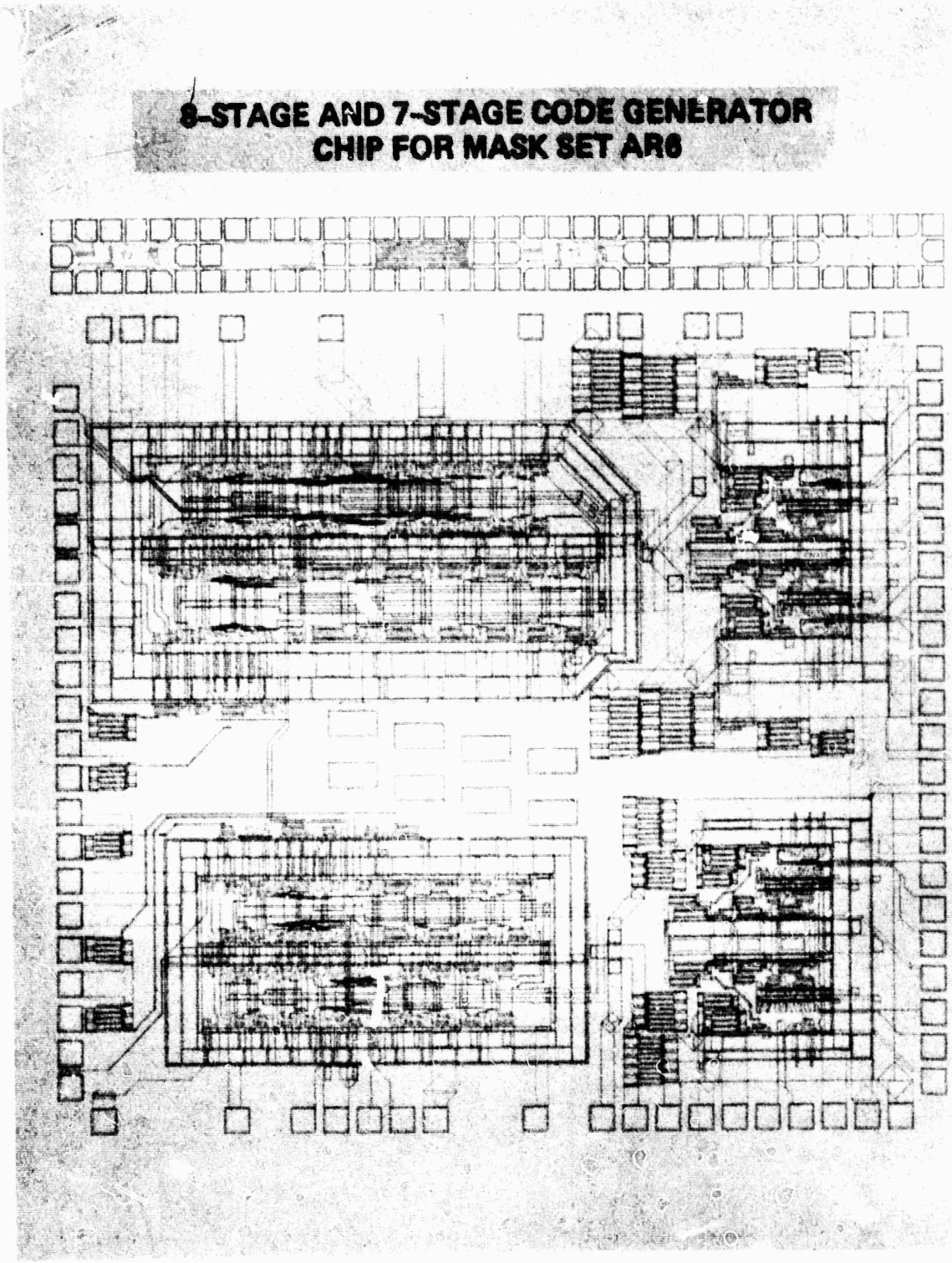


Fig. 4.1-2 Layout of the 8' stage and 7' stage code generators.

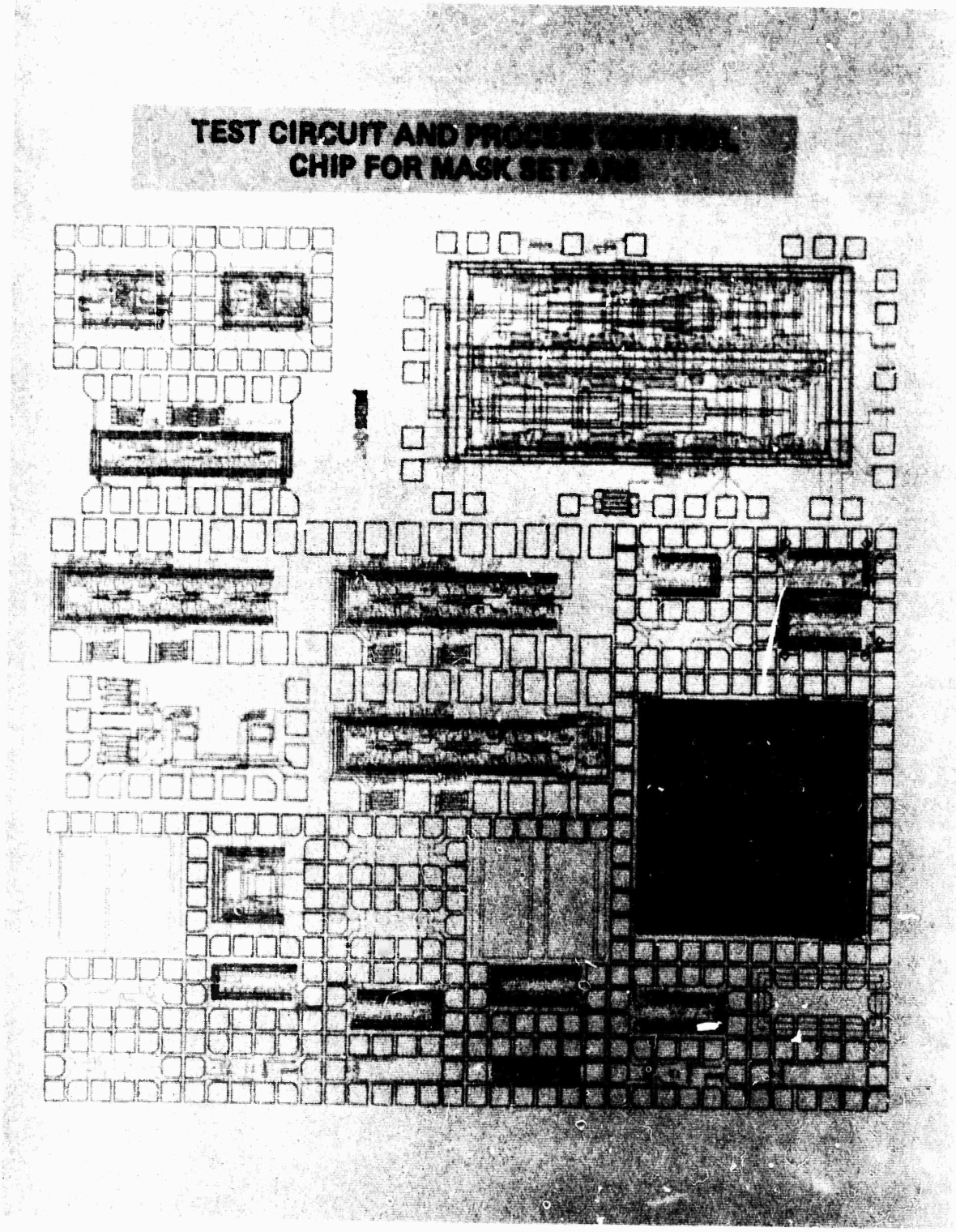


Fig. 4.1-3 Layout of the PCM chip containing process control and special test circuits.

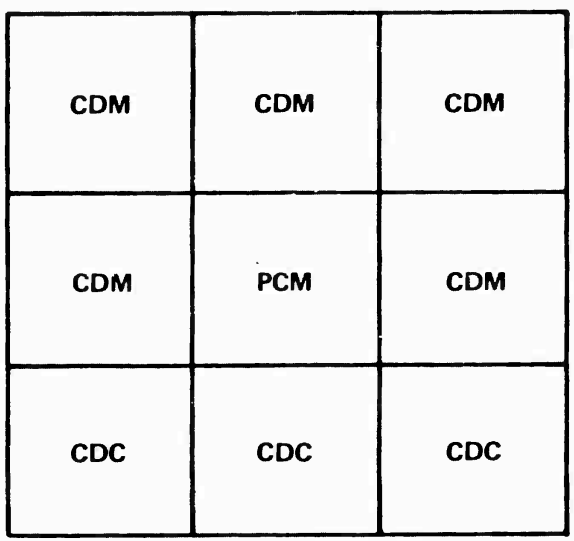


Fig. 4.1-4 Organization of the circuits on the AR6 mask set.

(CDM) chips, 12 code generator (CDC) chips, and 4 process control and test (PCM) chips.

An additional design feature has been incorporated in the AR6 mask set, so that it will provide fairly extensive yield data. Prior to the actual design of the multiplier, the anticipated chip area was small enough to result in a large number of chips per wafer, which would provide a substantial statistical data base. Once it was established that the area was as large as that of the AR5 multiplier, it became clear that the yield data obtained would be minimal, because not only would the large chip area increase the probability of a chip subtending a defect and failing, but it would also reduce the number of circuits, and thus the statistical significance of the data. If, however, the circuit were one-fourth the size, as originally anticipated, the greater likelihood of having a working part, and the increased number of circuits on the wafer would provide reasonable yield data. Also, the presence of clusters of two, three, and four adjacent working circuits would give an indication of the potential yield of larger circuits.

To facilitate obtaining the yield data, the layout of the multiplier was modified so that by changing only one mask layer--the second metal layer--the resultant circuit becomes four smaller multipliers, two 4 bit x 4 bit and two 4 bit x 3 bit. These four multipliers are independent with respect to all input, output, and power supply connections (except for the pad driver transistors), so that a short in one of them does not render the assemblage of four inoperative. The latches and one row of adders are left out; otherwise the adder array is the same as it would be for an 8 x 8 bit multiplier. Thus,

the size is shrunk by a factor of approximately four, and the desired yield data can be obtained.

The mask set was ordered with both versions of the second metal mask, one for 8 x 8 multipliers and one for the four smaller multipliers. The decision as to which wafers are processed into which multiplier need not be made until the last processing step, which is after the preliminary wafer probe (post Schottky metal). It is planned that initially most wafers will be processed as the four small multipliers to provide yield data.

The PCM arrangement is shown in Fig. 4.1-5. T1 and T2 occur twice, for wafer characterization. There are five ring oscillator configurations from earlier mask sets, electrical alignment structures, probe and crossover test structures, CV and linewidth test structures, and test gates.

The test circuits comprise: a shift register, similar to the seven stage code generator; a master/slave latch from the code generator; SD^2FL full adders, with and without the bit combining gate, from the multiplier; a divider implemented with Type D flip-flops; three versions of a divider implemented with OR/NAND two level logic gates to be used for maximum speed measurements.

4.2 MESFET Device Modeling

Two-dimensional numerical calculations have begun at North Carolina State University for the FET structure shown in Fig. 4.2-1. In order to verify the correctness of the numerical program, calculations were first made for a device with a uniformly doped channel with $N_d = 5 \times 10^{16}$ cm^{-3} and with a

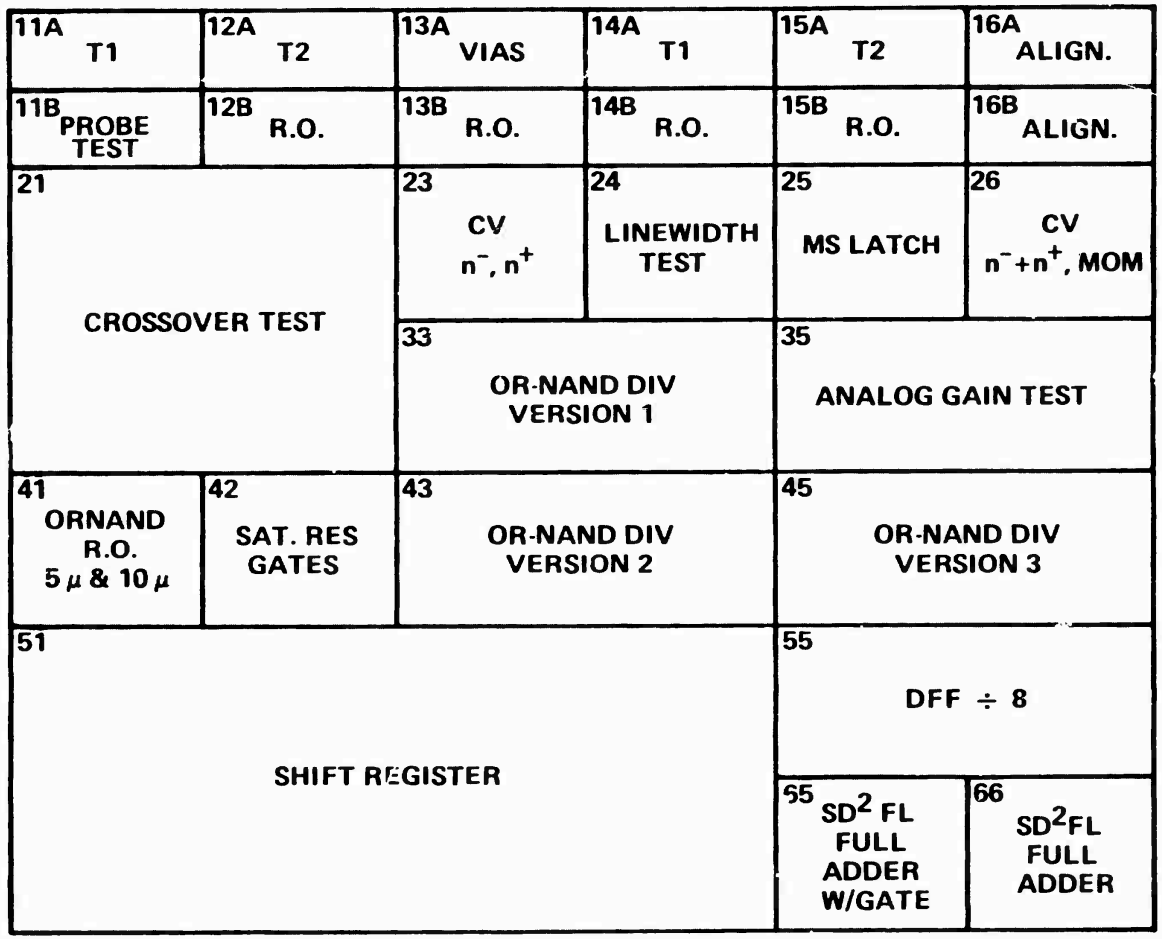


Fig. 4.1-5 Organization of the AR6-PCM test areas.

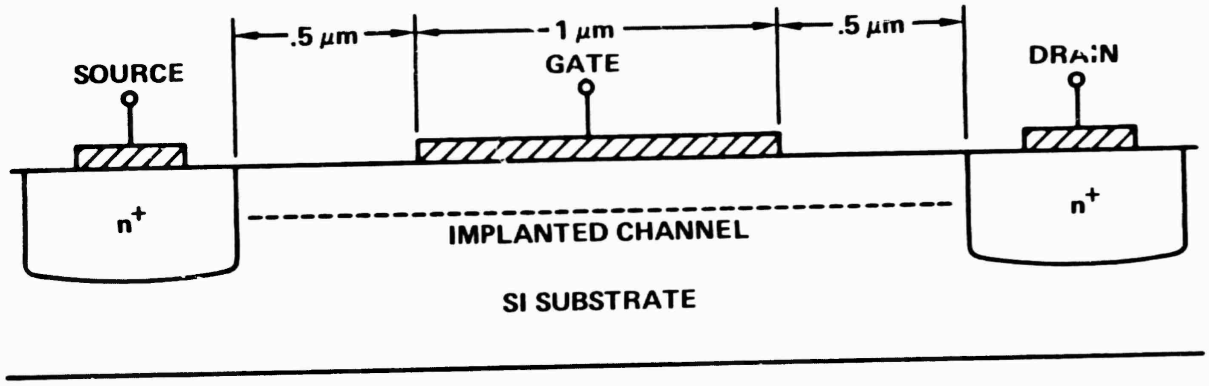


Fig. 4.2-1 FET structure.

depth of 0.16 μm. The calculated I-V characteristics are shown in Fig. 4.2-2. The results appear to be in reasonable agreement with the expected performance. The current saturation voltage is low as expected (1 V or less). The calculated I-V curves do not exhibit any negative resistance effects in contrast to some numerical calculations for GaAs FETs as reported by others.

The impurity profile in Fig. 4.2-3 was used next to simulate an implanted doping profile. The calculated I-V characteristics for this device are shown in Fig. 4.2-4 superimposed on the experimental data for a typical GaAs FET. The general shape of the calculated curves is seen to be in good agreement with the experimental data, especially with regard to the low pinchoff and low saturation voltage. Also, the magnitude of the calculated currents is in good agreement with the experimental data. The exact shape of the gate transfer curve is somewhat sensitive to the details of the doping profile, and the profile used in this calculation does not exactly match that of the experimental FET.

Gate capacitance values have been calculated for this FET at one bias condition and are reported below:

Bias conditions	V_{DS} = 2.5 V
	V_g = 0 V
Calculated capacitance	C_{gd} = 0.022 pF
	C_{gs} = 0.163 pF

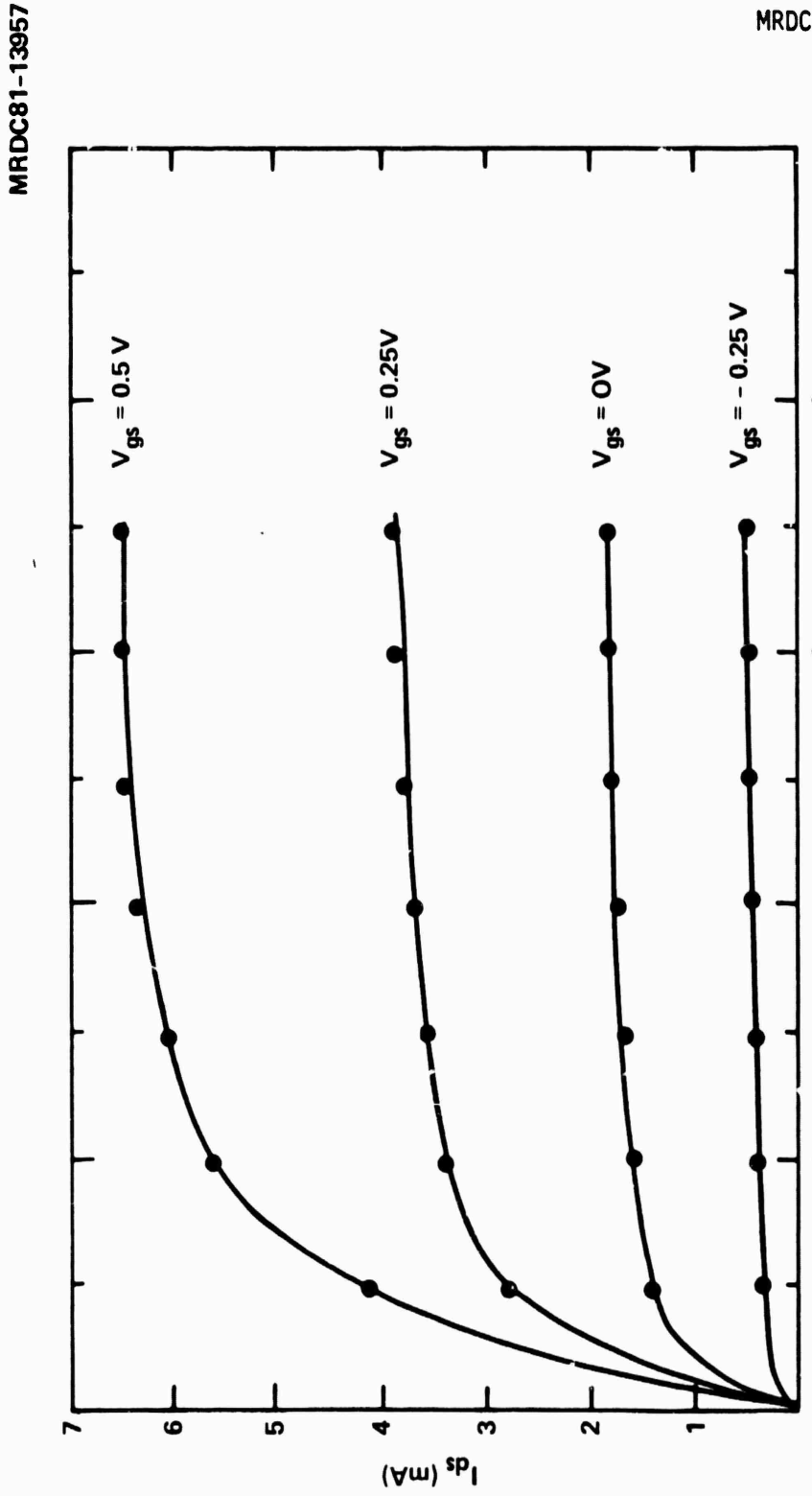


Fig. 4.2-2 I-V characteristics for Gaussian type impurity profile.

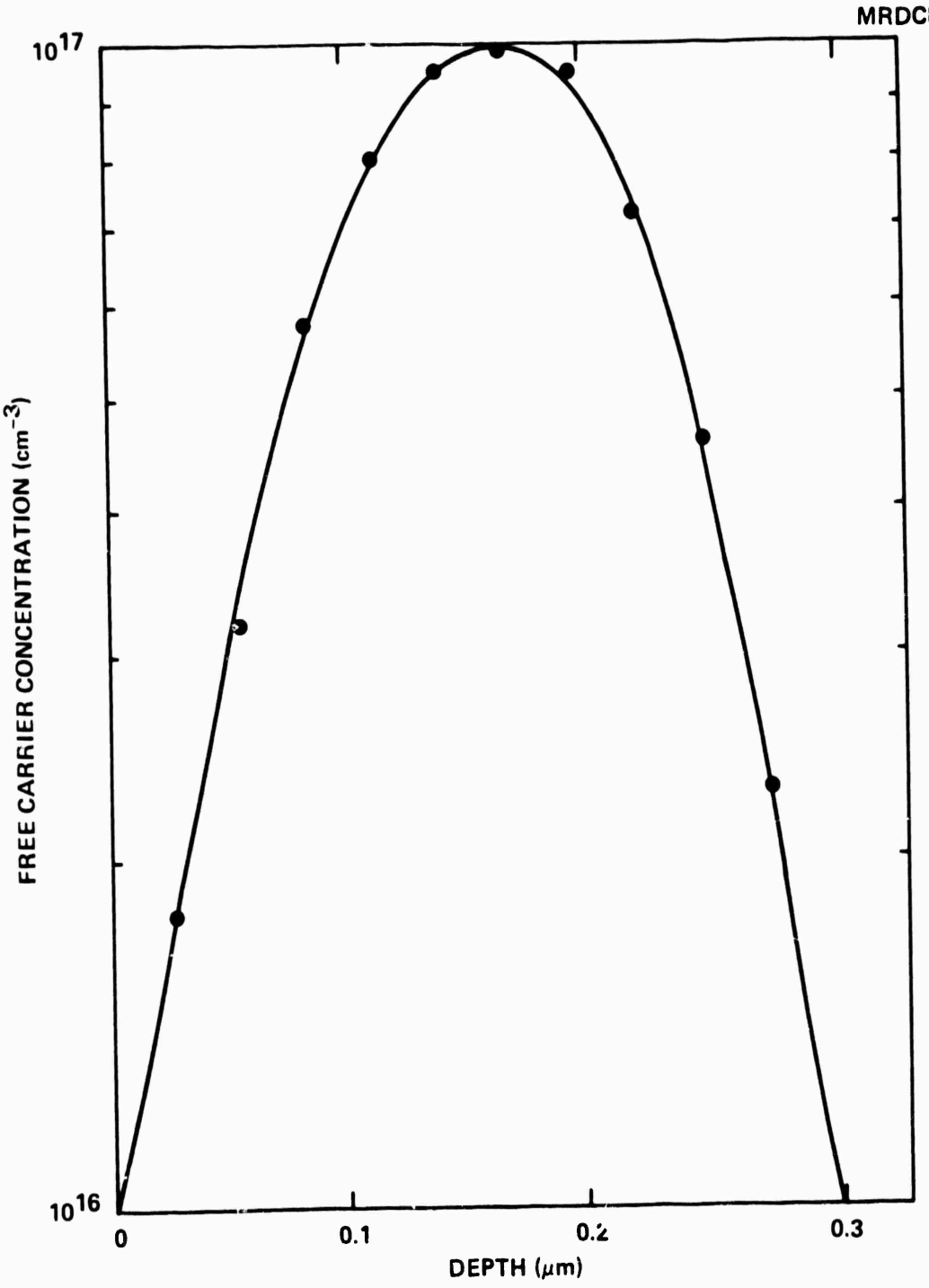
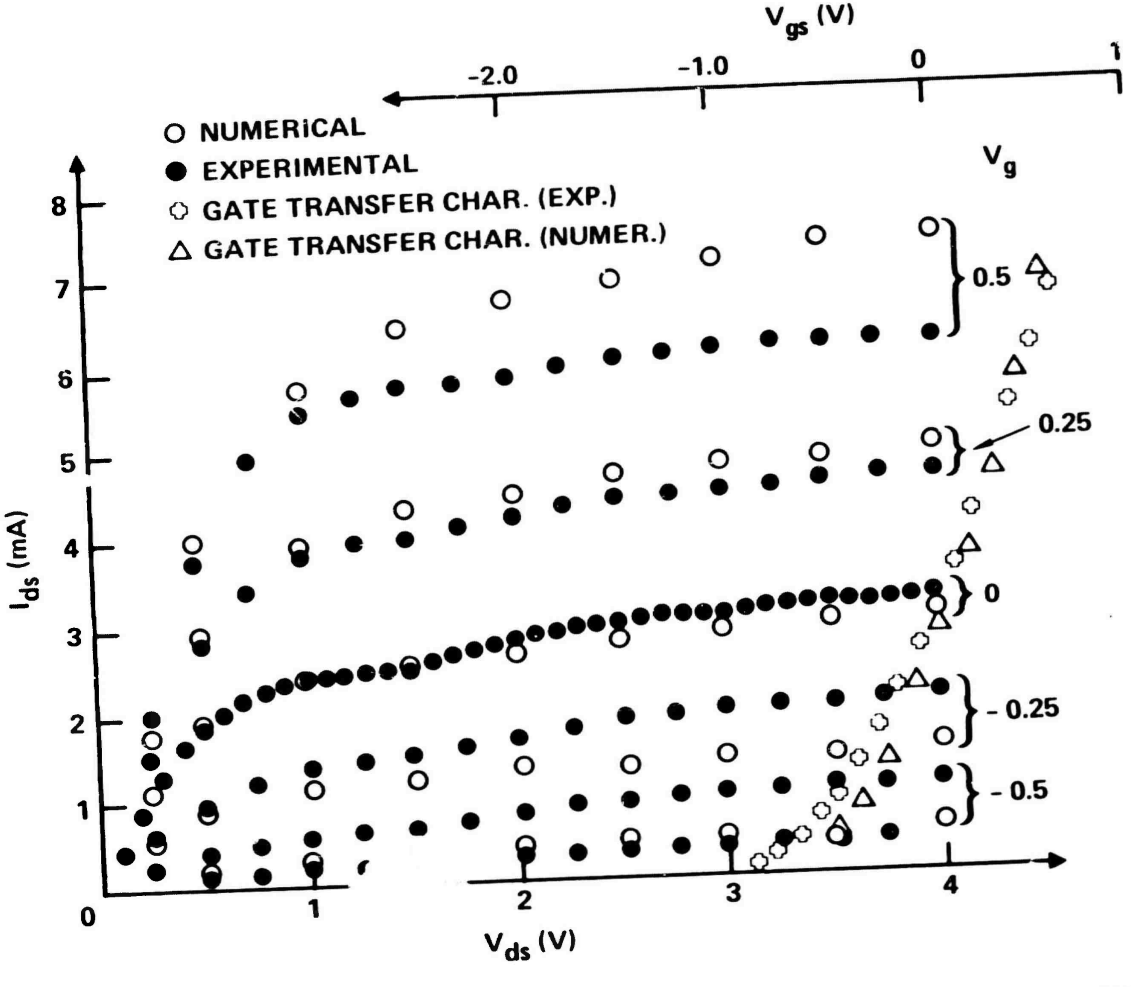


Fig. 4.2-3 Gaussian deoth type impurity profile for channel.



...I-V curves for actual implanted impurity profiles.

It should be noted that these values are the internal capacitance values and have not been corrected for the geometrical fringing capacitance of the gate and contact stripes above the device. This correction will increase both values but will have a larger percentage increase in the C_{gd} value.

Calculations are presently being made for FETs with impurity profiles more closely approximating the experimentally determined impurity profiles. Also, the small-signal calculations are being extended to include evaluations of g_m and g_{ds} to give a complete small-signal characterization of the FETs at all bias voltages. In addition the number of grid points used in the numerical simulation is being increased. The results of Fig. 4.2-4 were calculated with a 24 x 12 mesh of grid points. This mesh will be extended to about 60 x 20.

The two-dimensional FET models are continually being modified to improve them so that arbitrary contact locations and arbitrary doping profiles can be accommodated. Also, numerically efficient algorithms are being utilized so that the model can be used to examine in detail the electric field and charge concentration profiles in the device as a function of applied potentials. Currently the emphasis is on the static characteristics of the device. However, once that is completed, the model can be easily extended to the time dependent case for transient switching studies. Work on a two-dimensional Poisson solver has been completed. This solver obtains solutions for the position dependent potentials that are used in the continuity equation to obtain self-consistent solutions. Work is currently progressing on integrating the Poisson solver with a SOR solution of the continuity equation.

Monte Carlo Analysis

The objective of this work, also carried out at North Carolina State University, is to use Monte Carlo simulation to correct the results of two-dimensional device analysis. The latter uses simplified, static models for the dependence of mobility and diffusion coefficient on electric field. Consequently, the field profile and charge distribution obtained from a standard device analysis program are not necessarily self-consistent. On the other hand, a Monte Carlo simulation automatically includes the correct μ-E and D-E relations and forces $E(x,y)$ and $\rho(x,y)$ to be consistent.

The approach is as follows: a two-dimensional device analysis program is used to obtain initial values $E_0(x,y)$. These are passed to a two-dimensional Monte Carlo program, which calculates (by simulation) a charge distribution $\rho_0(x,y)$. This is used in Poisson's equation to obtain a new field profile $E_1(x,y)$. The revised $E_1(x,y)$ is passed back to the Monte Carlo program where a new charge distribution $\rho_1(x,y)$ is calculated. This is used in Poisson's equation to obtain a new field profile $E_2(x,y)$. This process is repeated until reasonably self-consistent $E(x,y)$ and $\rho(x,y)$ are obtained.

For large (> 1 μm) devices, the correction provided by the Monte Carlo simulation may not be significant. Standard device analysis programs give results that are in reasonable agreement with experiment (measured drain source characteristics). For small (< 1 μm) devices the correction may be significant, especially for low operating voltages, because of velocity overshoot and other effects not accounted for in standard device analysis programs.

An existing Monte Carlo program has been modified to include a two-dimensional electric field (n x m points) and to compile a charge distribution $\rho(x,y)$ (n x m points). The program is now being tested.

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